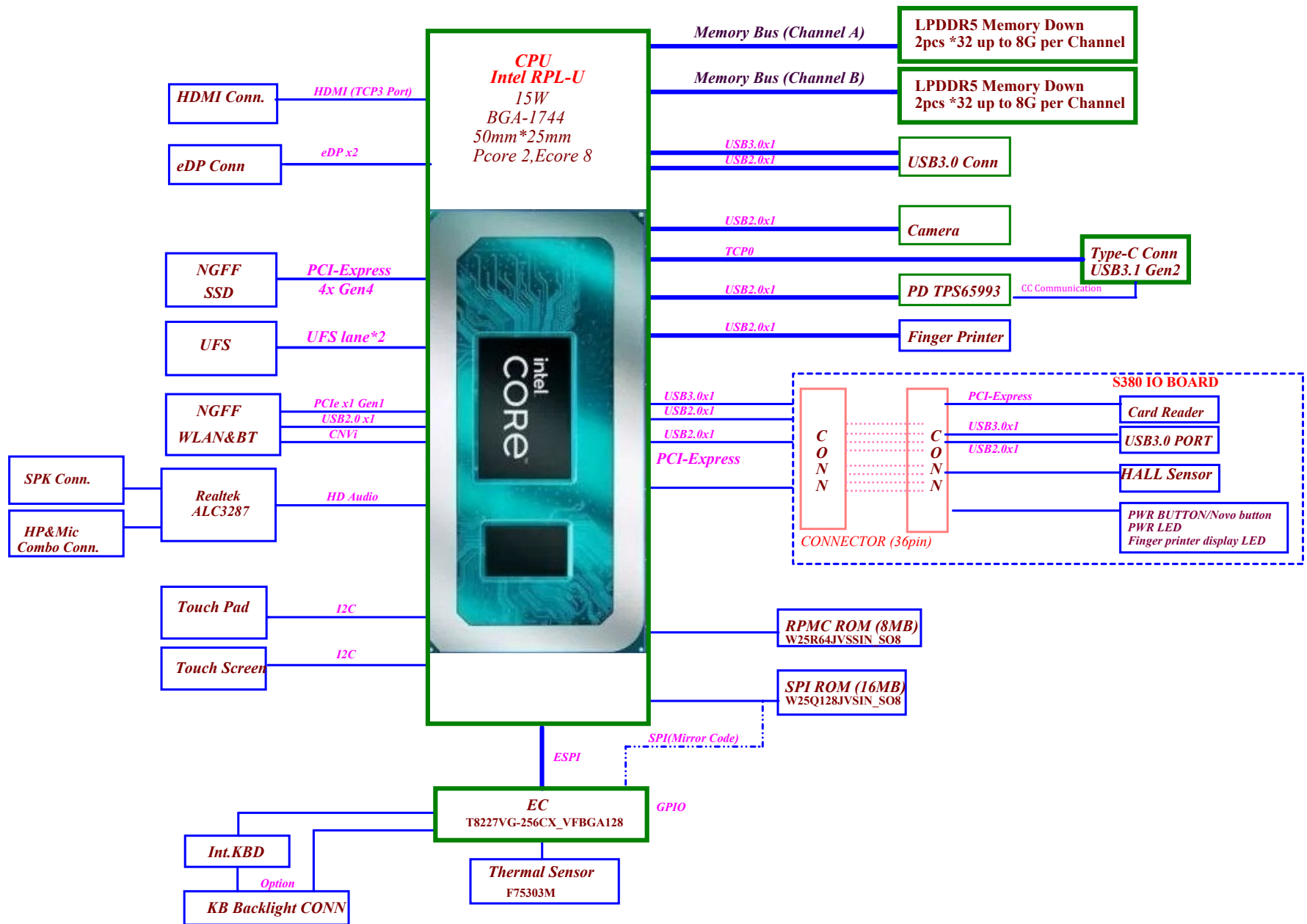


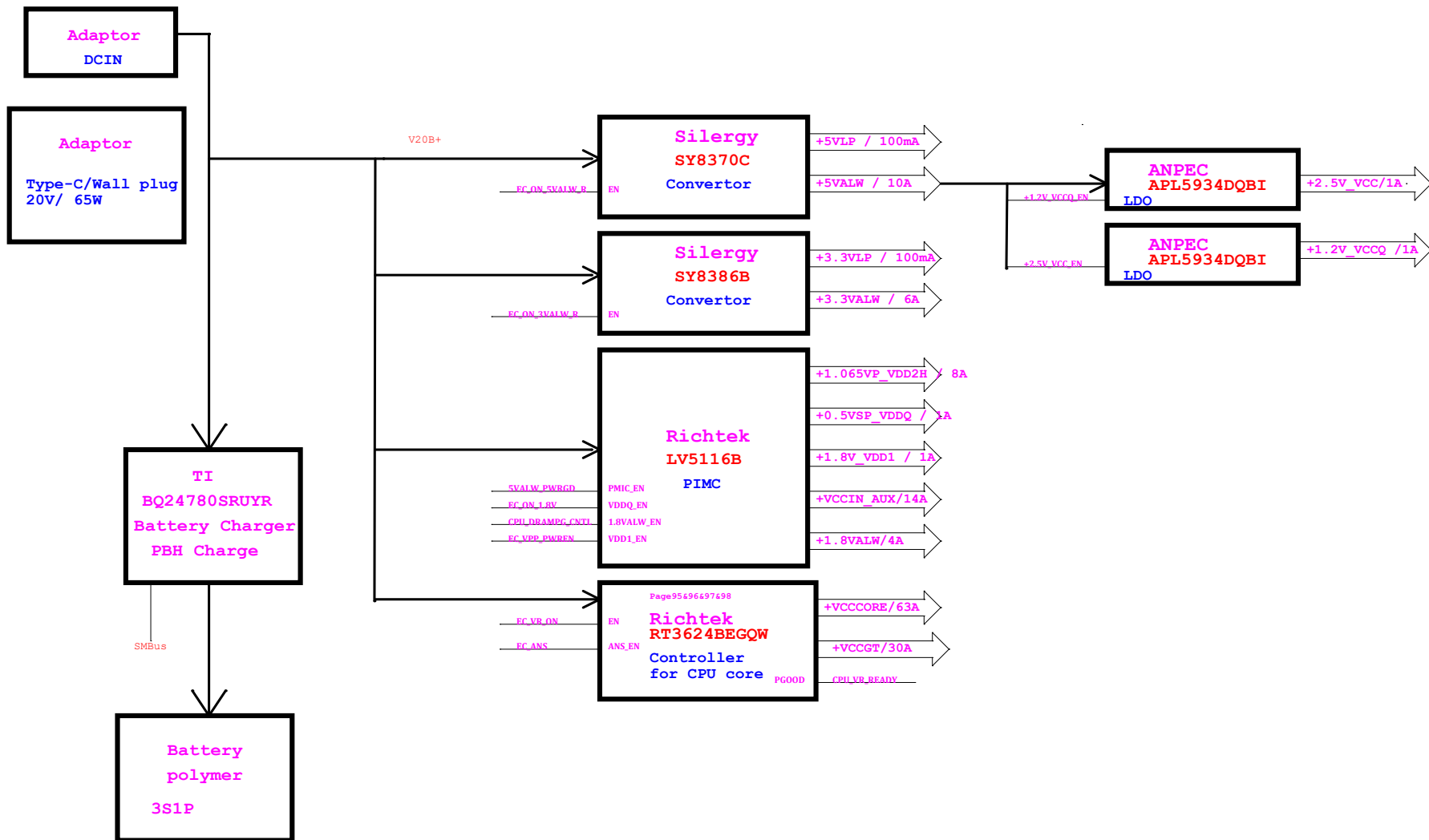
LCFC NM-F331

KS485 MB Schematics Document

Raptor Lake U15W with LPDDR5

REV: 0.1
2023-01-23





Voltage Rails (O --> Means ON , X --> Means OFF)

<div>Power Plane</div> <div>State</div>				
	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

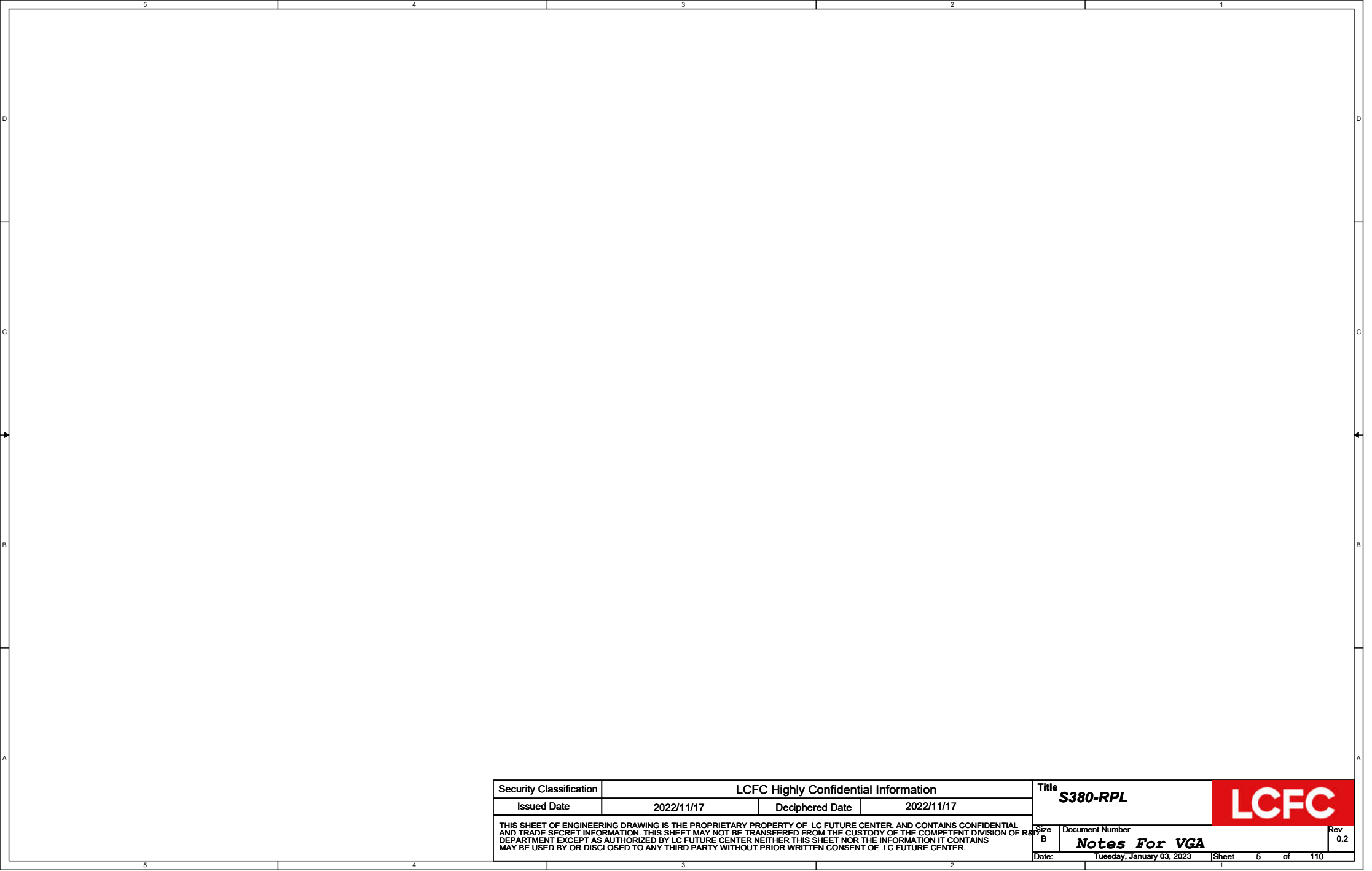
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF


HSIO PORT	Function
USB3.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 USB3.0 intel debug conn
	4 NC
USB2.0	1 USB3.0 Conn DB
	2 Type-c USB2.0
	3 NC
	4 NC
	5 NC
	6 FP
	7 NC
	8 Camera
	9 USB3.0 Conn MB
	10 Bluetooth
PCH PCIE	5~6 NC
	7 WLAN
	8 Card Reader
	9~10 UFS
	11 NC
	12 NC
CPU PCIE	X4_A PCIE SSD
	X4_B NC
	X8 NC

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WinMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address		EC SMBus2 address		EC SMBus3 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	not use		DDR4 SODIMM	need to update
Charger	0001 0010 b	PCH	need to update			WLAN	Reserved
SPU PWR Controller need to update						DGPU	need to update



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					B	Notes For VGA	0.2
Date:					Tuesday, January 03, 2023	Sheet	5 of 110

Virtual Symbol

PCB

CPU

GPU

DRAM MD&
BOARD ID

DRAM X76

VRAM&
BOARD ID

VRAM X76

UFS

RTC X76

Virtual Symbol_Power

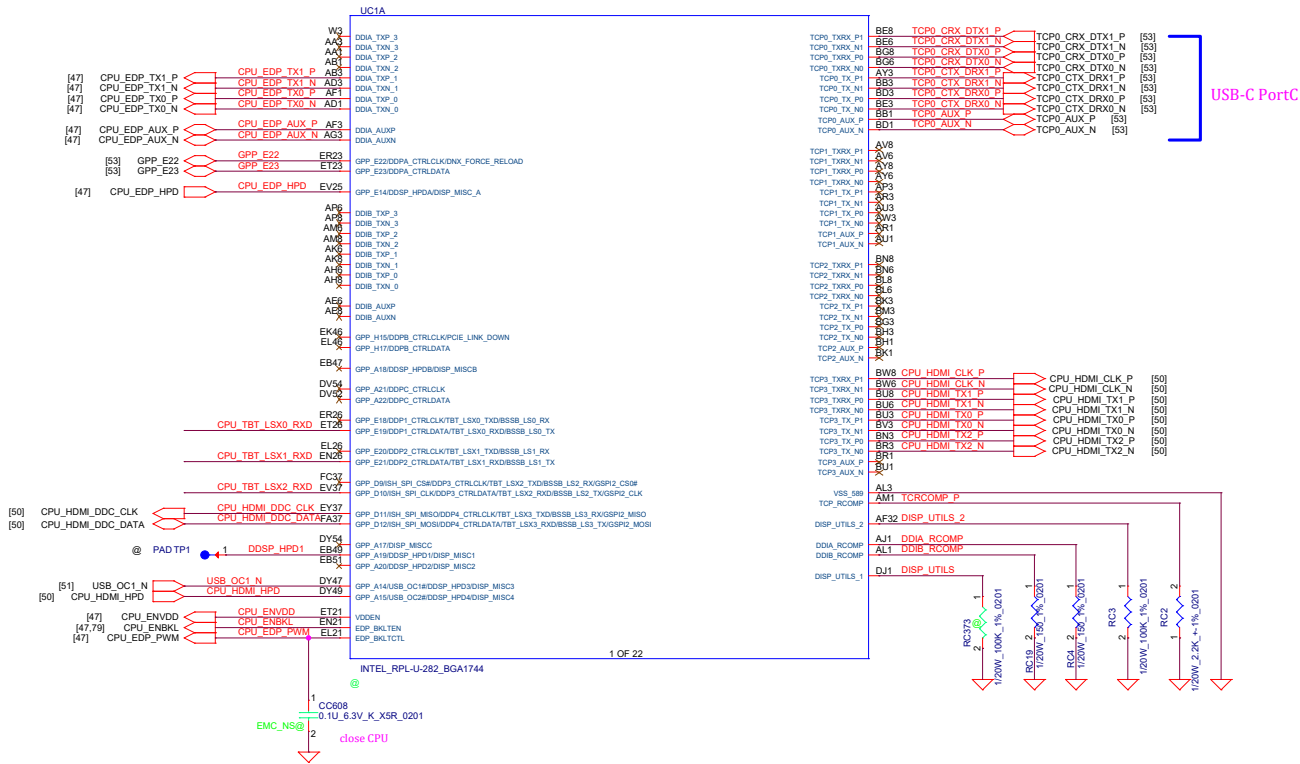
15W

HDMI Royalty

BOM Structure

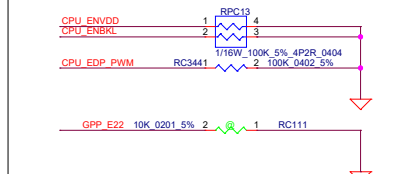
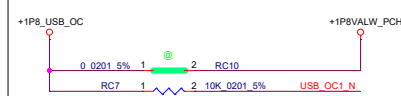
BOM Structure	Description
8	00-stuff
FHD8	For FHD Panel Part
HDR8	For HDR Panel Part
L48	For L48/R part
L58	For J5778 Part
L68	For J5778 Part
8M ROM8	For 8G 8108 ROM part
AMP8	For external Amplifier solution part
AMP_N58	For external Amplifier solution us-stuff part
AMP_PWR8	For discrete Amplifier power solution part
ANS8	For power ANS solution part
USM8	For power USM solution part
BL8	For Key Board Backlight part
CD8	For C Host Board
CHANNELA8	For Memory Channel A part
DDPA8	For Memory Channel A ROP part
SDPA8	For Memory Channel A ROP part
DDPB8	For Memory Channel B ROP part
SDPB8	For Memory Channel B ROP part
	For RF1 Phase part
MP8	For MP Phase Part
PCIE48	For PCIe Gen4 part
EMC8	For EMC part
EMC_158	For ETV31 EMC part
EMC_N58	For EMC us-stuff part
RF_N58	For RF us-stuff part
AOAC8	For AOAC part
CNV18	For CNV1 WLAN part
ME8	For ME part
OPT8	For 8V GPU part
OPTN168	For NV 168-GB GPU part
OPTN178	For NV 178-GB GPU part
TS8	For touch screen part
TP8	For Touch Pad Part
UMA8	For UMA part

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				Notes For BOM	



Design Notice

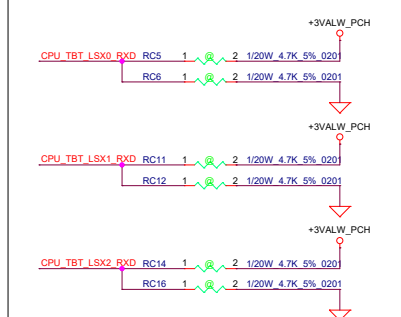
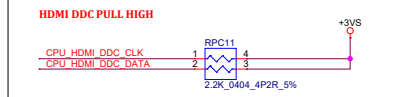
USB3/USB2 Port Pairing for USB-C Connectors				
	TCP0	TCP1	TCP2	TCP3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6



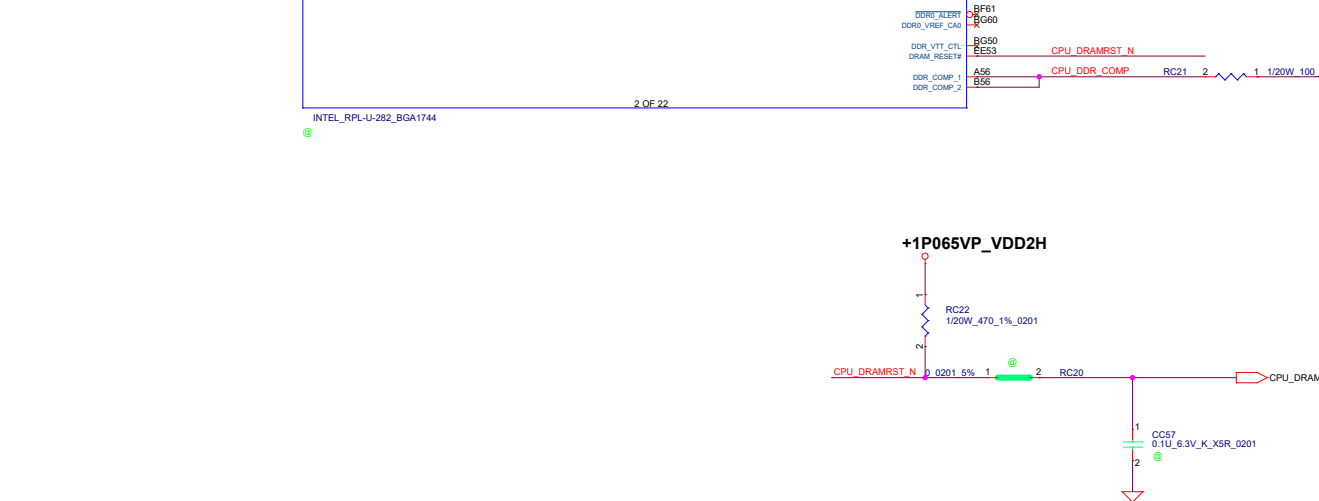
For Glitch Free
Cap or pull-down resistor is required depending on panel power sequencing spec or power delivery

Option 1:Cap Implementation
330 nF for 3.3V Ramp Rate from 5-50ms
33 nF for 3.3V Ramp Rate Less than 5ms

Option 2:Pull-down Resistor Implementation
100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode



TBT LSX RXD:
DDP12C /TBT LSX /BBSB LS pins VCC configuration
Rising edge of RSMRST#
This strap has a 20 kohm \pm 30% internal pull-down.
0 = DDP 12C / TBT LSX / BBSB LS pins at 1.8V
1 = DDP 12C / TBT LSX / BBSB LS pins at 3.3V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



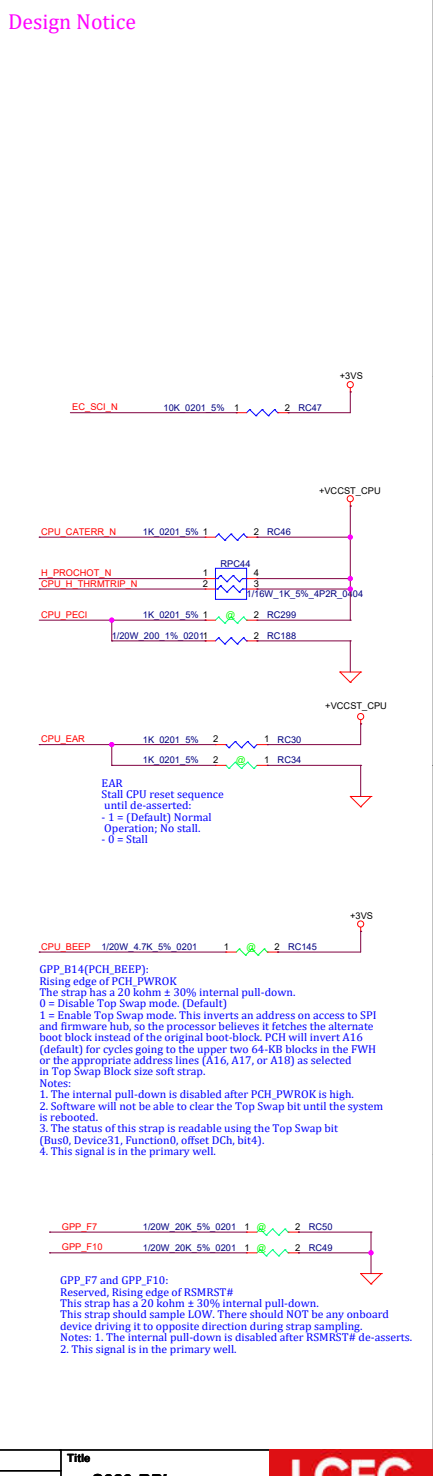
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Issued Date	2022/11/17	Deciphered Date	2022/11/17	
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			Date 2022/11/17	Drawn 002




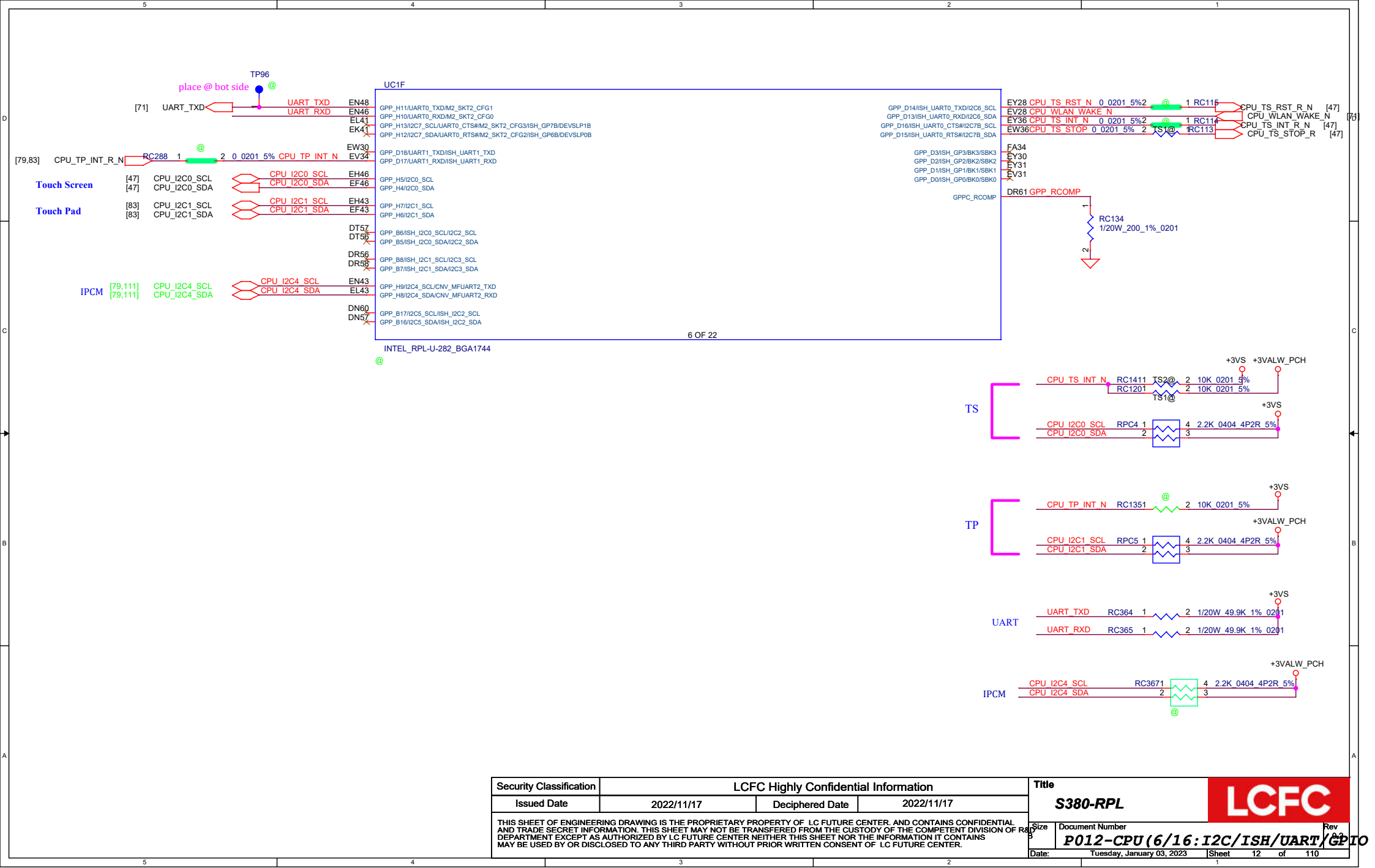
UD3 Clock

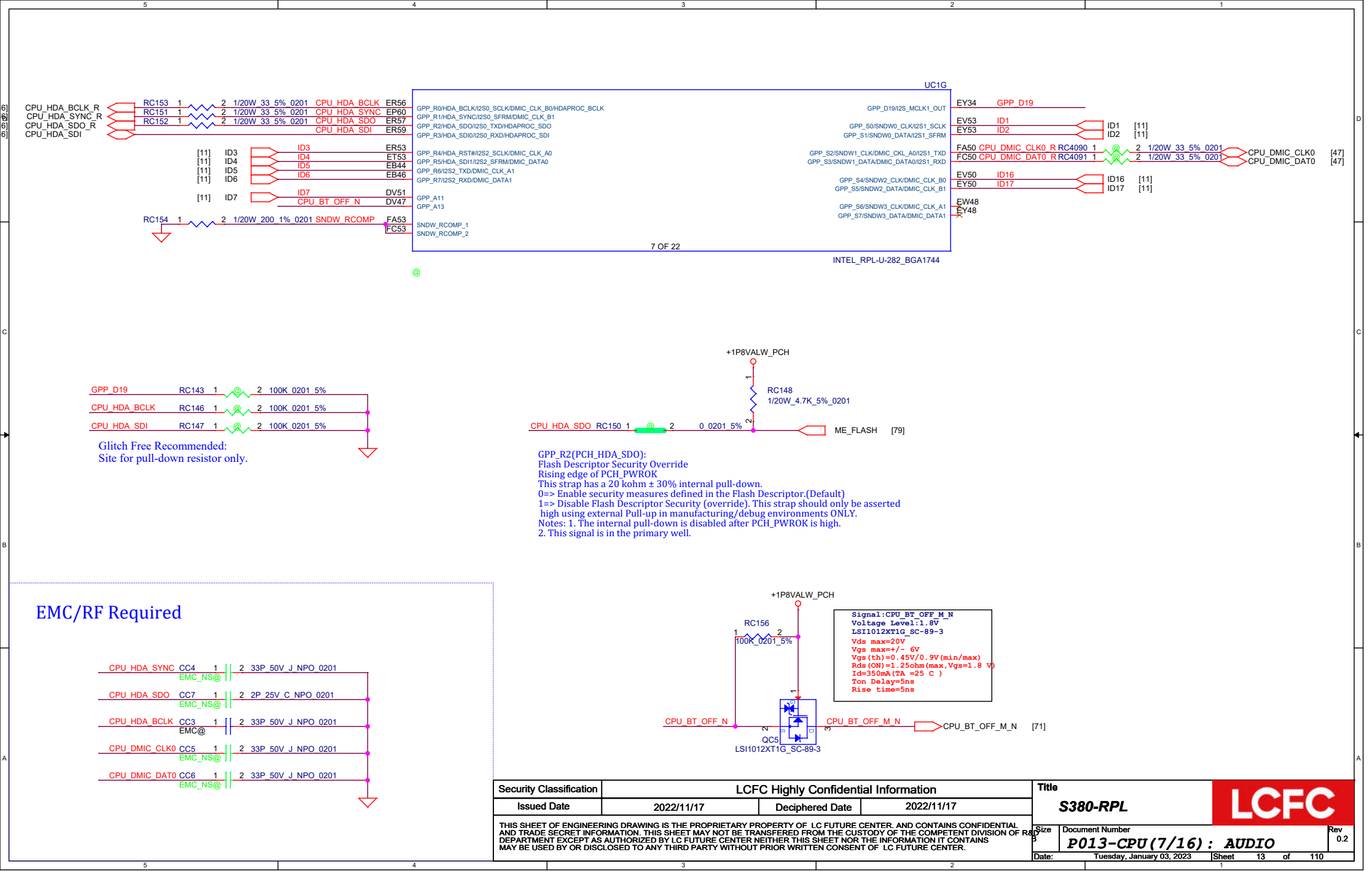
UD4 Clock

EMC/RF Required



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Size	Document Number			Rev	
	P010-CPU(4/16): SMC/JTAG			0.2	
Date:	Tuesday, January 03, 2023			Sheet	10 of 110





Note: Need care the DB board
PCIE TX/PX signal connection
Card Reader

WLAN

USB3.2 Debug Port3

USB3.2 DB Port1

USB3.2 PORT1

SSD
PCIEX4_A (PEG60)

This signal can be left open if PCIeX4_A/B interface is Power gated.

PCIEX4_B (PEG62)

9 OF 22

INTEL_RPL-U-282_BGA1744

UC1H

PCIEX8 (PEG10) Gen5

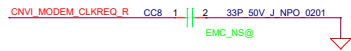
This signal can be left open if PCIeX8 interface is Not use

8 OF 22

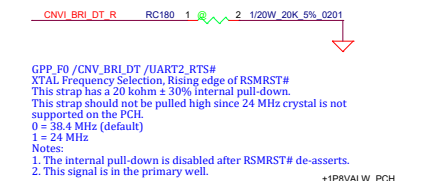
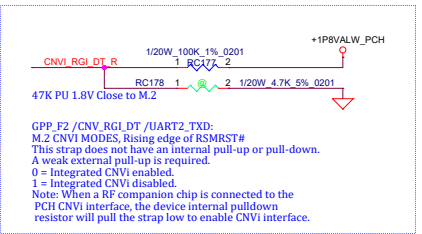
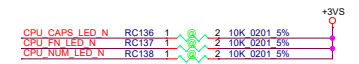
INTEL_RPL-U-282_BGA1744

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					P014-CPU(8/16) : PCIE/USB/SATA
				Date	Tuesday, January 03, 2023

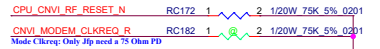
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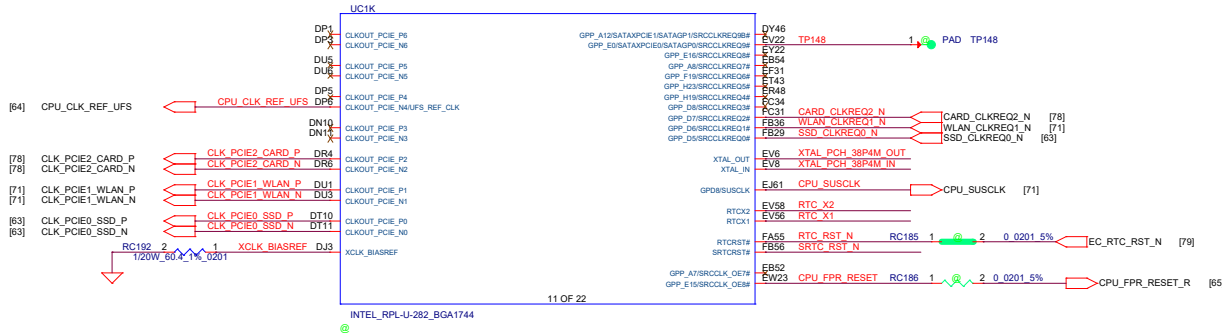
Design Notice



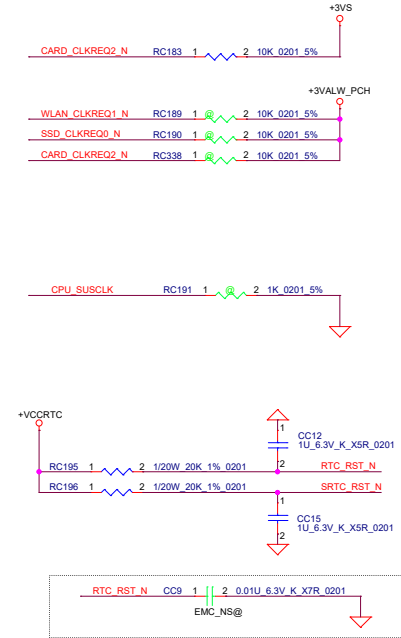
Glitch Free Requirements:
Pull-down resistor to ensure the stability of the signal during platform bootup



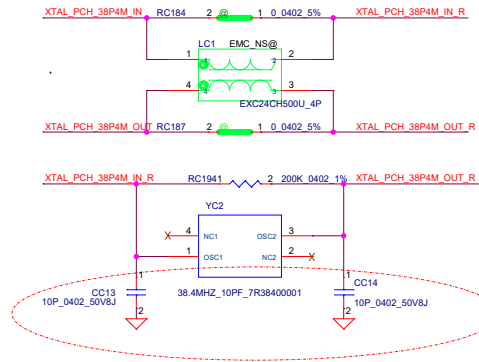
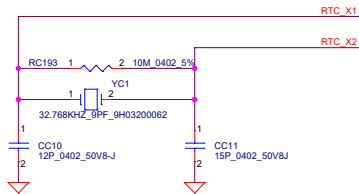
PCI Express® Clock Output: Serial Reference 100 MHz PCIe® specification
compliant differential output clocks to PCIe® devices
CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe® Gen1, Gen2, and Gen3 support.
CLKOUT_PCIE_P/N [4, 3, 0] = PCIe Gen4 and PCIe Gen5 support must use these ports.

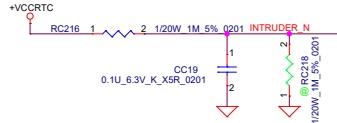
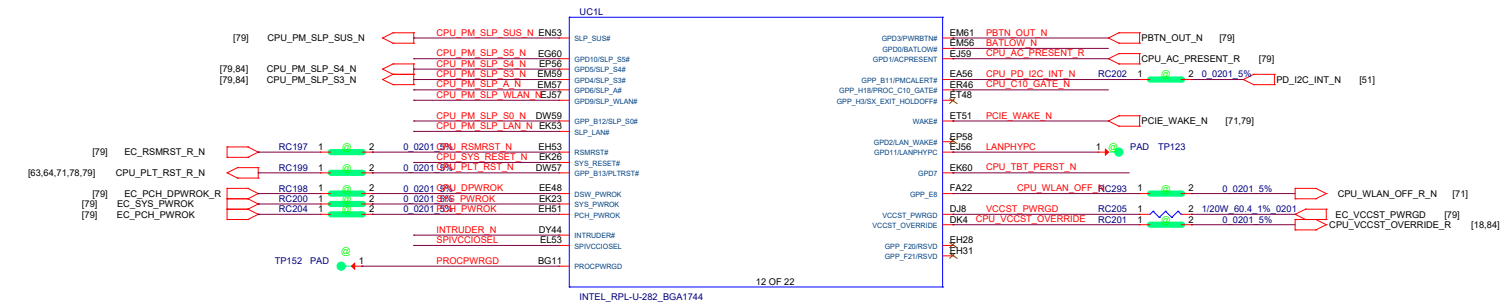


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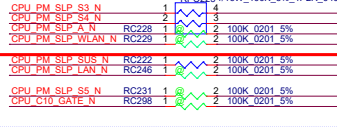
Crystal





INTRUDER#
RTC-Well Input Strap Requirements
should have a weak external pull-up to VccRTC

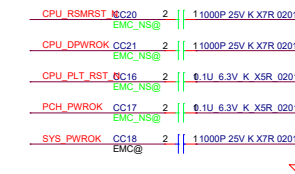
Glitch



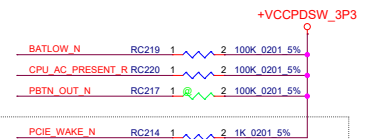
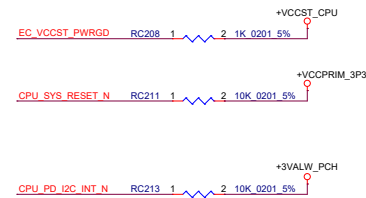
Glitch Free Requirements:
Pull-up resistor is required if a device is monitoring SLP_S0#
before RSMRST# de-assertion

100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode

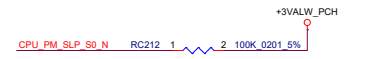
EMC/RF Required



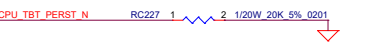
Design Notice



POCIE_WAKE_N
Integrated pull-down 15K ~ 40K;
Pull-down is configurable and can be enabled in Deep Sx state;
An external pull-up resistor is required.

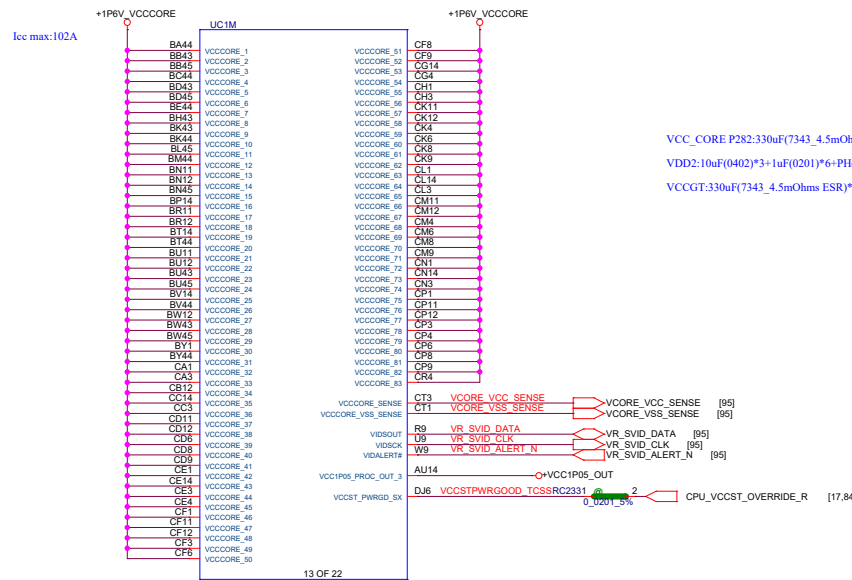


SPIVCCIOSEL:
SPI Operation Voltage Select
Rising edge of DSW_PWR0K
There is no internal pull-up or pull-down on the strap. An
external resistor is required.
0 = SPI voltage is 3.3V (4.7 kohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K pull-up to DSW_PWR0K)



GPD7(BB_TBT_PERST#):
Reserved
Rising edge of DSW_PWR0K
This signal has a 20K+-30% internal pull-down.
This strap should sample LOW. There should NOT be any on-board device
driving it to opposite direction during strap sampling
Notes:
1. The internal pull-down is disabled after DSW_PWR0K is high.
2. This signal is in the DSW well

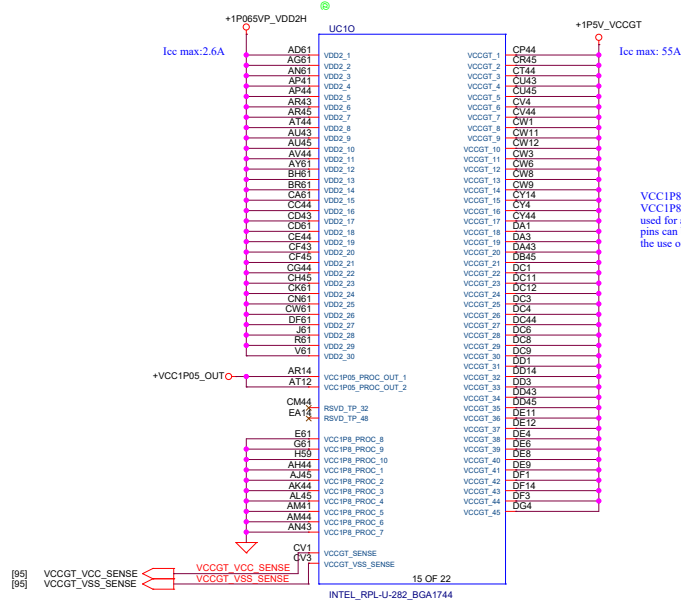
Design Notice



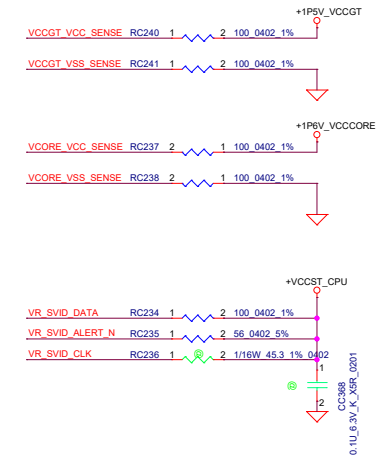
VCC_CORE P282:330uF(7343 4.5mOhms ESR)*2+47uF(0603)*7+2.2uF(0402)*8

VDD2:10uF(0402)*3+1uF(0201)*6+PH(0402)*2

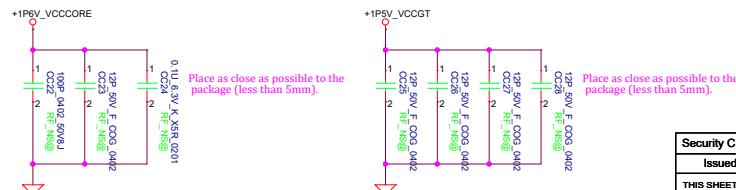
VCCGT:330uF(7343 4.5mOhms ESR)*2+47uF(0603)*7+PH(0603)*1+22uF(0402)*8+10uF(0402)*2+PH(0402)*2



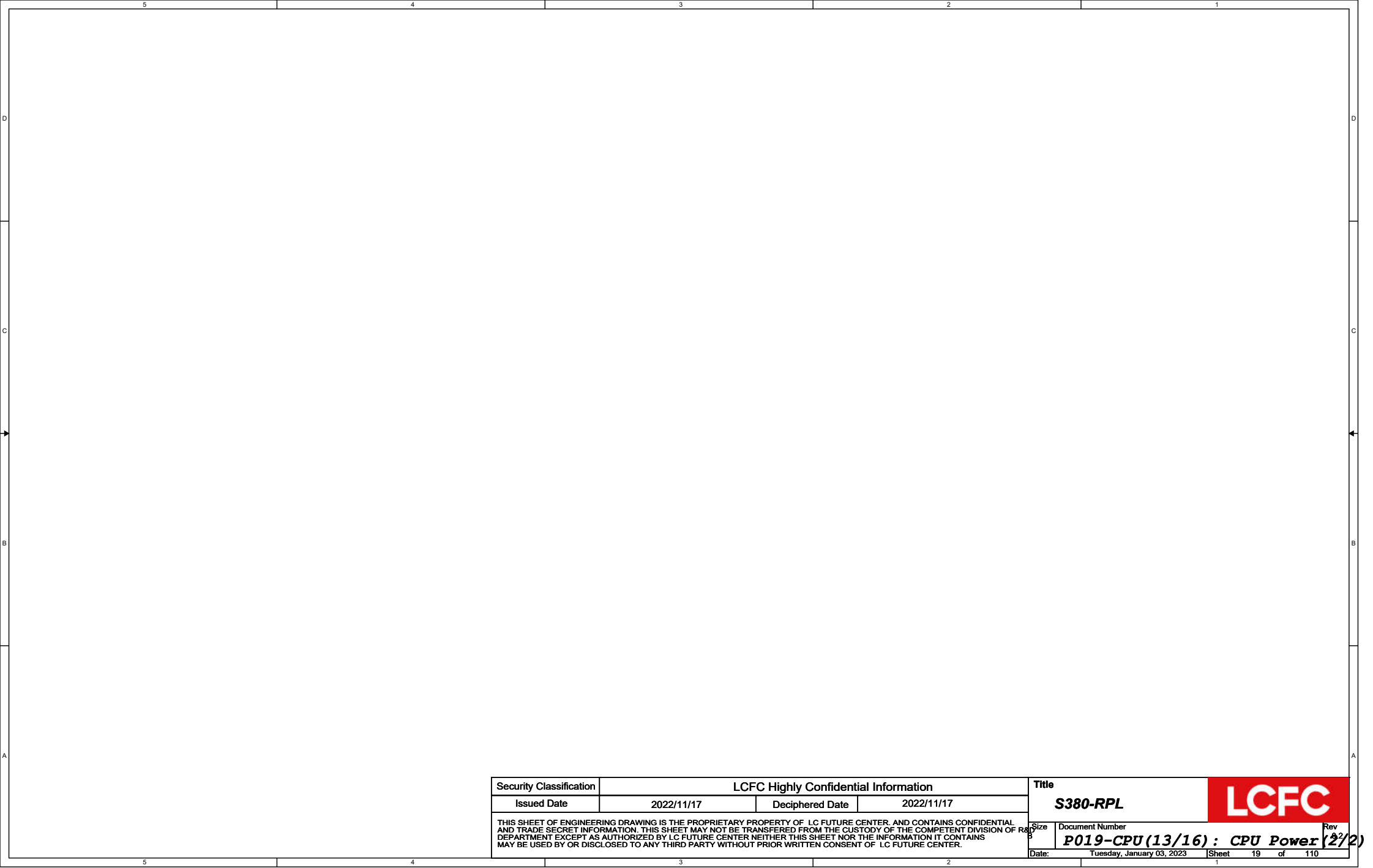
VCC1P8_PROC is the 1.8V rail for PCIe x8-PEG10 capable of PCIe Gen5 speed. VCC1P8_PROC pins are only related to PCIe x8-PEG10, if PEG10 port is not used for any PCIe Gen speed and if disabled the PEG10 in FIT tool than these pins can be connected to GND. Processor PCIe 010 can be disabled through the use of FIT tool.



EMC/RF Required



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Date	10/22/2022	January 18, 2023	Sheet	18	of	110	



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				3	P019-CPU(13/16) : CPU Power	Rev 2/
				Date:	Tuesday, January 03, 2023	Sheet 19 of 110

P019-CPU(13/16) : CPU Power (2²/2)

UC1P		
A3	V88.7	V88.74
A10	V88.1	V88.75
A21	V88.2	V88.76
A22	V88.3	V88.77
A25	V88.4	V88.78
A26	V88.5	V88.79
A28	V88.6	V88.80
A30	V88.7	V88.81
A31	V88.8	V88.82
A33	V88.9	V88.83
A40	V88.10	V88.84
A47	V88.11	V88.85
A53	V88.12	V88.86
A60	V88.13	V88.87
AA11	V88.14	V88.88
AA21	V88.15	V88.89
AA26	V88.16	V88.90
AA31	V88.17	V88.91
AA35	V88.18	V88.92
AA40	V88.19	V88.93
AA44	V88.20	V88.94
AA57	V88.21	V88.95
AA59	V88.22	V88.96
AB16	V88.23	V88.97
AB21	V88.24	V88.98
AB26	V88.25	V88.99
AB31	V88.26	V88.100
AB35	V88.27	V88.101
AB44	V88.28	V88.102
AC4	V88.29	V88.103
AC10	V88.30	V88.104
AC44	V88.31	V88.105
AC51	V88.32	V88.106
AC55	V88.33	V88.107
AC6	V88.34	V88.108
AD21	V88.35	V88.109
AD26	V88.36	V88.110
AD31	V88.37	V88.111
AD35	V88.38	V88.112
AD46	V88.39	V88.113
AD48	V88.40	V88.114
AD58	V88.41	V88.115
AE12	V88.42	V88.116
AE17	V88.43	V88.117
AE22	V88.44	V88.118
AE27	V88.45	V88.119
AE32	V88.46	V88.120
AE37	V88.47	V88.121
AE40	V88.48	V88.122
AE44	V88.49	V88.123
AE52	V88.50	V88.124
AE9	V88.51	V88.125
AF4	V88.52	V88.126
AF46	V88.53	V88.127
AG1	V88.54	V88.128
AG51	V88.55	V88.129
AG55	V88.56	V88.130
AG58	V88.57	V88.131
AH9	V88.58	V88.132
AJ3	V88.59	V88.133
AJ41	V88.60	V88.134
AJ47	V88.61	V88.135
AJ49	V88.62	V88.136
AJ54	V88.63	V88.137
AK20	V88.64	V88.138
AK25	V88.65	V88.139
AK30	V88.66	V88.140
AK37	V88.67	V88.141
AK39	V88.68	V88.142
AK4	V88.69	V88.143
AK7	V88.70	V88.144
AK9	V88.71	V88.145
AK9	V88.72	V88.146
AK9	V88.73	V88.147
AK9	V88.74	V88.148

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UC1Q		
BF58	V88.149	V88.222
BG12	V88.150	V88.223
BG44	V88.151	V88.224
BG52	V88.152	V88.225
BG9	V88.153	V88.226
BH4	V88.154	V88.227
BH46	V88.155	V88.228
BH48	V88.156	V88.229
BH59	V88.157	V88.230
BH59	V88.158	V88.231
BH59	V88.159	V88.232
BH59	V88.160	V88.233
BH59	V88.161	V88.234
BH59	V88.162	V88.235
BH59	V88.163	V88.236
BH59	V88.164	V88.237
BH59	V88.165	V88.238
BH59	V88.166	V88.239
BH59	V88.167	V88.240
BH59	V88.168	V88.241
BH59	V88.169	V88.242
BH59	V88.170	V88.243
BH59	V88.171	V88.244
BH59	V88.172	V88.245
BH59	V88.173	V88.246
BH59	V88.174	V88.247
BH59	V88.175	V88.248
BH59	V88.176	V88.249
BH59	V88.177	V88.250
BH59	V88.178	V88.251
BH59	V88.179	V88.252
BH59	V88.180	V88.253
BH59	V88.181	V88.254
BH59	V88.182	V88.255
BH59	V88.183	V88.256
BH59	V88.184	V88.257
BH59	V88.185	V88.258
BH59	V88.186	V88.259
BH59	V88.187	V88.260
BH59	V88.188	V88.261
BH59	V88.189	V88.262
BH59	V88.190	V88.263
BH59	V88.191	V88.264
BH59	V88.192	V88.265
BH59	V88.193	V88.266
BH59	V88.194	V88.267
BH59	V88.195	V88.268
BH59	V88.196	V88.269
BH59	V88.197	V88.270
BH59	V88.198	V88.271
BH59	V88.199	V88.272
BH59	V88.200	V88.273
BH59	V88.201	V88.274
BH59	V88.202	V88.275
BH59	V88.203	V88.276
BH59	V88.204	V88.277
BH59	V88.205	V88.278
BH59	V88.206	V88.279
BH59	V88.207	V88.280
BH59	V88.208	V88.281
BH59	V88.209	V88.282
BH59	V88.210	V88.283
BH59	V88.211	V88.284
BH59	V88.212	V88.285
BH59	V88.213	V88.286
BH59	V88.214	V88.287
BH59	V88.215	V88.288
BH59	V88.216	V88.289
BH59	V88.217	V88.290
BH59	V88.218	V88.291
BH59	V88.219	V88.292
BH59	V88.220	V88.293
BH59	V88.221	V88.294

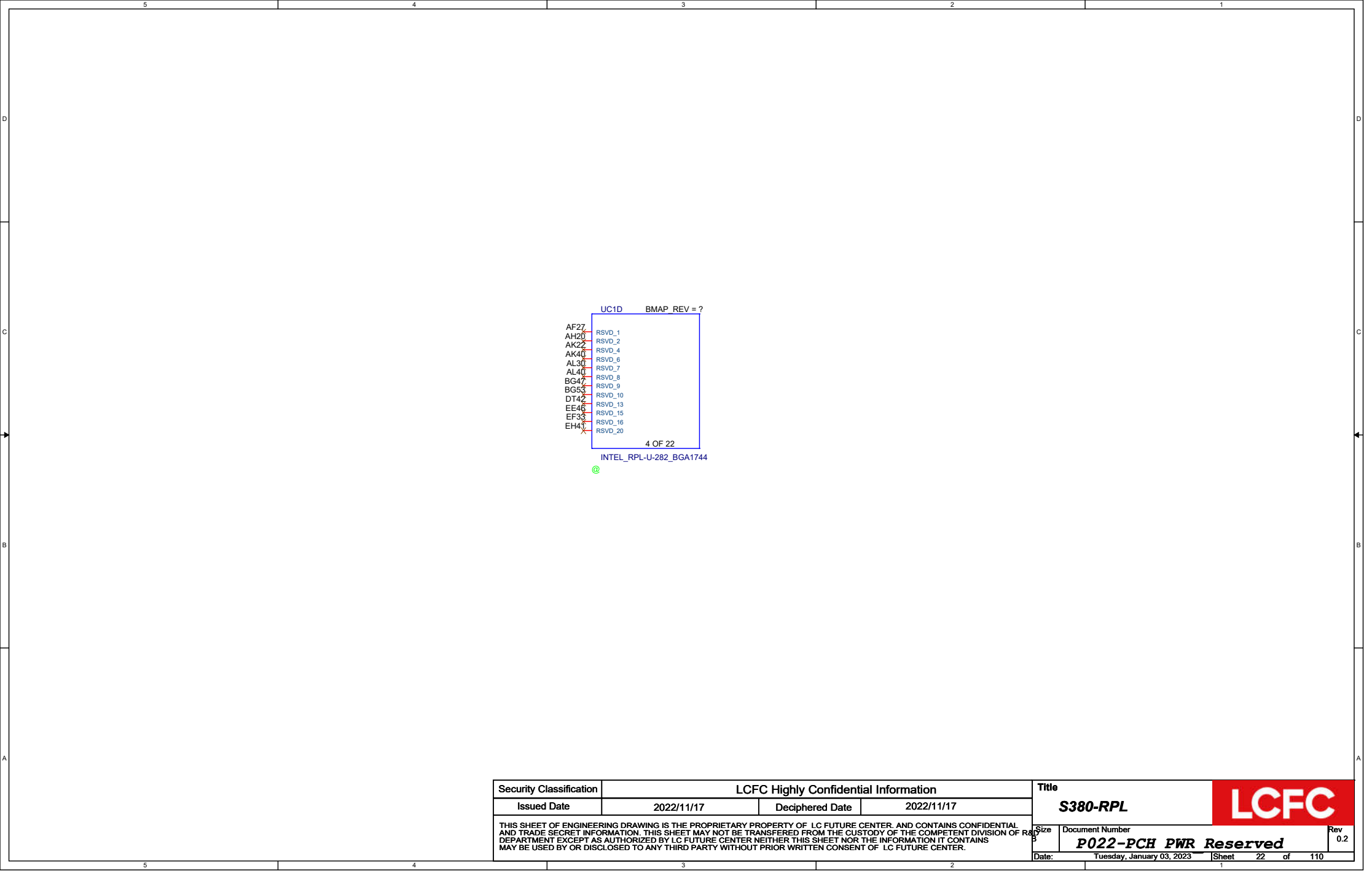
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UC1R		
CD47	V88.295	V88.365
CD54	V88.296	V88.370
CD57	V88.297	V88.371
CD59	V88.298	V88.372
DE44	V88.299	V88.373
DE51	V88.299	V88.374
DE55	V88.300	V88.375
DE55	V88.301	V88.376
DE55	V88.302	V88.377
DE55	V88.303	V88.378
DE55	V88.304	V88.379
DE55	V88.305	V88.380
DE55	V88.306	V88.381
DE55	V88.307	V88.382
DE55	V88.308	V88.383
DE55	V88.309	V88.384
DE55	V88.310	V88.385
DE55	V88.311	V88.386
DE55	V88.312	V88.387
DE55	V88.313	V88.388
DE55	V88.314	V88.389
DE55	V88.315	V88.390
DE55	V88.316	V88.391
DE55	V88.317	V88.392
DE55	V88.318	V88.393
DE55	V88.319	V88.394
DE55	V88.320	V88.395
DE55	V88.321	V88.396
DE55	V88.322	V88.397
DE55	V88.323	V88.398
DE55	V88.324	V88.399
DE55	V88.325	V88.400
DE55	V88.326	V88.401
DE55	V88.327	V88.402
DE55	V88.328	V88.403
DE55	V88.329	V88.404
DE55	V88.330	V88.405
DE55	V88.331	V88.406
DE55	V88.332	V88.407
DE55	V88.333	V88.408
DE55	V88.334	V88.409
DE55	V88.335	V88.410
DE55	V88.336	V88.411
DE55	V88.337	V88.412
DE55	V88.338	V88.413
DE55	V88.339	V88.414
DE55	V88.340	V88.415
DE55	V88.341	V88.416
DE55	V88.342	V88.417
DE55	V88.343	V88.418
DE55	V88.344	V88.419
DE55	V88.345	V88.420
DE55	V88.346	V88.421
DE55	V88.347	V88.422
DE55	V88.348	V88.423
DE55	V88.349	V88.424
DE55	V88.350	V88.425
DE55	V88.351	V88.426
DE55	V88.352	V88.427
DE55	V88.353	V88.428
DE55	V88.354	V88.429
DE55	V88.355	V88.430
DE55	V88.356	V88.431
DE55	V88.357	V88.432
DE55	V88.358	V88.433
DE55	V88.359	V88.434
DE55	V88.360	V88.435
DE55	V88.361	V88.436
DE55	V88.362	V88.437
DE55	V88.363	V88.438
DE55	V88.364	V88.439
DE55	V88.365	V88.440
DE55	V88.366	V88.441
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DE55	V88.370	V88.445

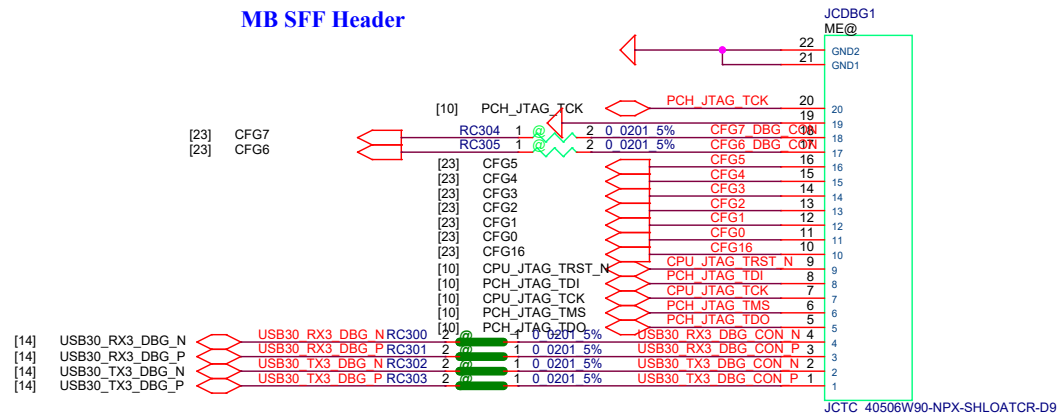
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INTEL_RPL-U-282_BGA1744

UC1S		
F56	V88.443	V88.517
F59	V88.444	V88.518
F59	V88.445	V88.519
F59	V88.446	V88.520
F59	V88.447	V88.521
F59	V88.448	V88.522
F59	V88.449	V88.523
F59	V88.450	V88.524
F59	V88.451	V88.525
F59	V88.452	V88.526
F59	V88.453	V88.527
F59	V88.454	V88.528
F59	V88.455	V88.529
F59	V88.456	V88.530
F59	V88.457	V88.531
F59	V88.458	V88.532
F59	V88.459	V88.533
F59	V88.460	V88.534
F59	V88.461	V88.535
F59	V88.462	V88.536
F59	V88.463	V88.537
F59	V88.464	V88.538
F59	V88.465	V88.539
F59	V88.466	V88.540
F59	V88.467	V88.541
F59	V88.468	V88.542
F59	V88.469	V88.543
F59	V88.470	V88.544
F59	V88.471	V88.545
F59	V88.472	V88.546
F59	V88.473	V88.547
F59	V88.474	V88.548
F59	V88.475	V88.549
F59	V88.476	V88.550
F59	V88.477	V88.551
F59	V88.478	V88.552
F59	V88.479	V88.553
F59	V88.480	V88.554
F59	V88.481	V88.555
F59	V88.482	V88.556
F59	V88.483	V88.557
F59	V88.484	V88.558
F59	V88.485	V88.559
F59	V88.486	V88.560
F59	V88.487	V88.561
F59	V88.488	V88.562
F59	V88.489	V88.563
F59	V88.490	V88.564
F59	V88.491	V88.565
F59	V88.492	V88.566
F59	V88.493	V88.567
F59	V88.494	V88.568
F59	V88.495	V88.569
F59	V88.496	V88.570
F59	V88.497	V88.571
F59	V88.498	V88.572
F59	V88.499	V88.573
F59	V88.500	V88.574
F59	V88.501	V88.575
F59	V88.502	V88.576
F59	V88.503	V88.577
F59	V88.504	V88.578
F59	V88.505	V88.579
F59	V88.506	V88.580
F59	V88.507	V88.581
F59	V88.508	V88.582
F59	V88.509	V88.583
F59	V88.510	V88.584
F59	V88.511	V88.585
F59	V88.512	V88.586
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F59	V88.516	V88.590

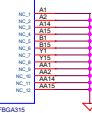
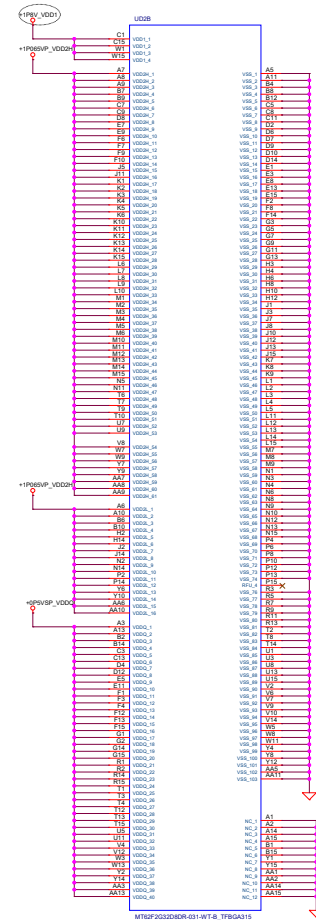
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				5	P022-PCH PWR Reserved	0.2	
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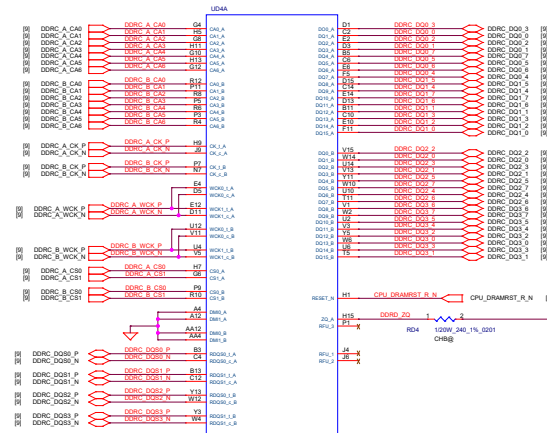


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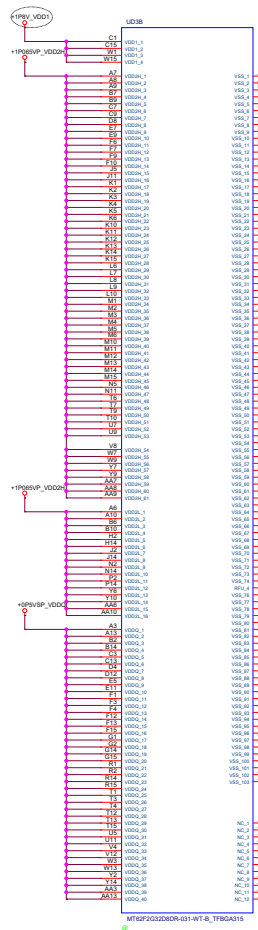




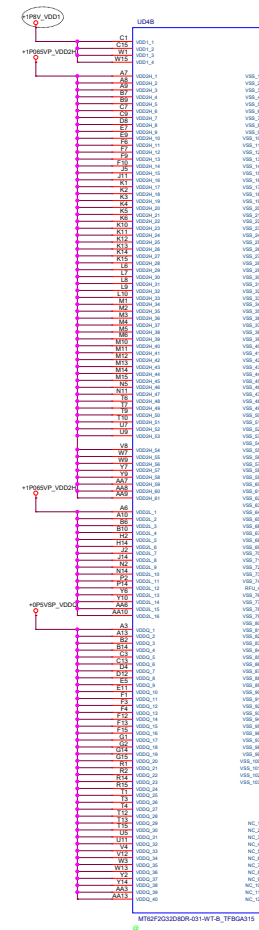
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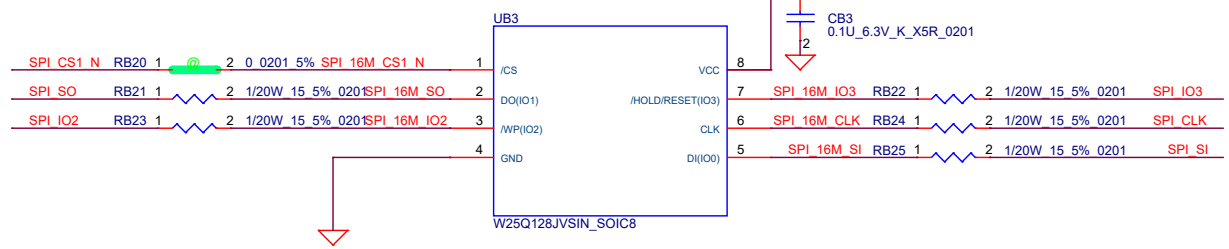
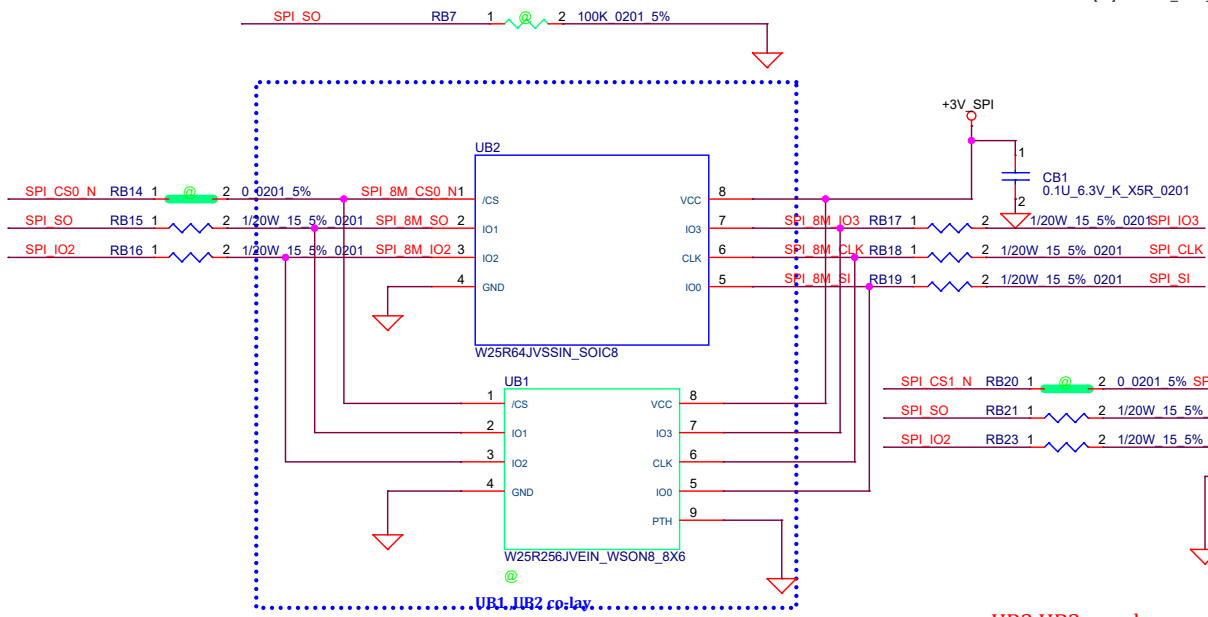
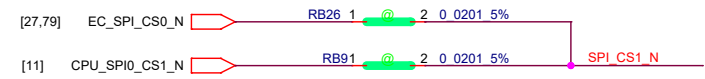
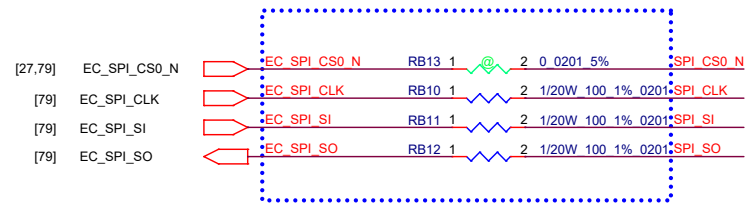
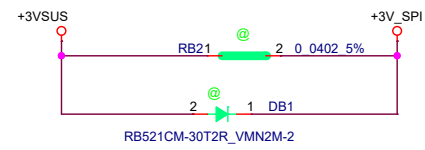
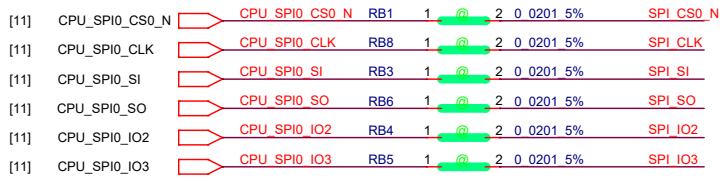
MT67P322DNR-01-WT-B_TPBGA15



MT67P322DNR-01-WT-B_TPBGA15



MT67P322DNR-01-WT-B_TPBGA15



UB2 UB3 are changed FROM IQ to IN by common pool

Change list:
Remove GPU Circuit

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					B	P029-GPU Display Interface	0.2	
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Remove GPU Circuit

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				Date:	Tuesday, January 03, 2023	Sheet	30	of 113

Change list:
Remove GPU Circuit

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Size		Document Number		Rev					
B		P031-GPU MEM Interface (C/D)		0.2					
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					B	P032-GPU GPIO/JTAG			
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				Date:	Tuesday, January 03, 2023	Sheet	33	of 113

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Remove GPU Circuit

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					B	P034-GPU PWR1	0.2				
					Date:	Tuesday, January 03, 2023		Sheet	34	of	113

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Remove GPU Circuit

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										B	P035-GPU PWR2	0.2			
										Date:	Tuesday, January 03, 2023	Sheet	35	of	113

Change list:
Remove GPU Circuit

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					B	P036-GPU GND		0.2
					Date:	Tuesday, January 03, 2023		Sheet

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Remove GPU Circuit

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					B	VRAM A [64:32]	0.2	
					Date:	Tuesday, January 03, 2023	Sheet 37 of 113	


Change list:
Remove GPU Circuit

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				Date:	Tuesday, January 03, 2023	Sheet 38 of 113

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Remove GPU Circuit

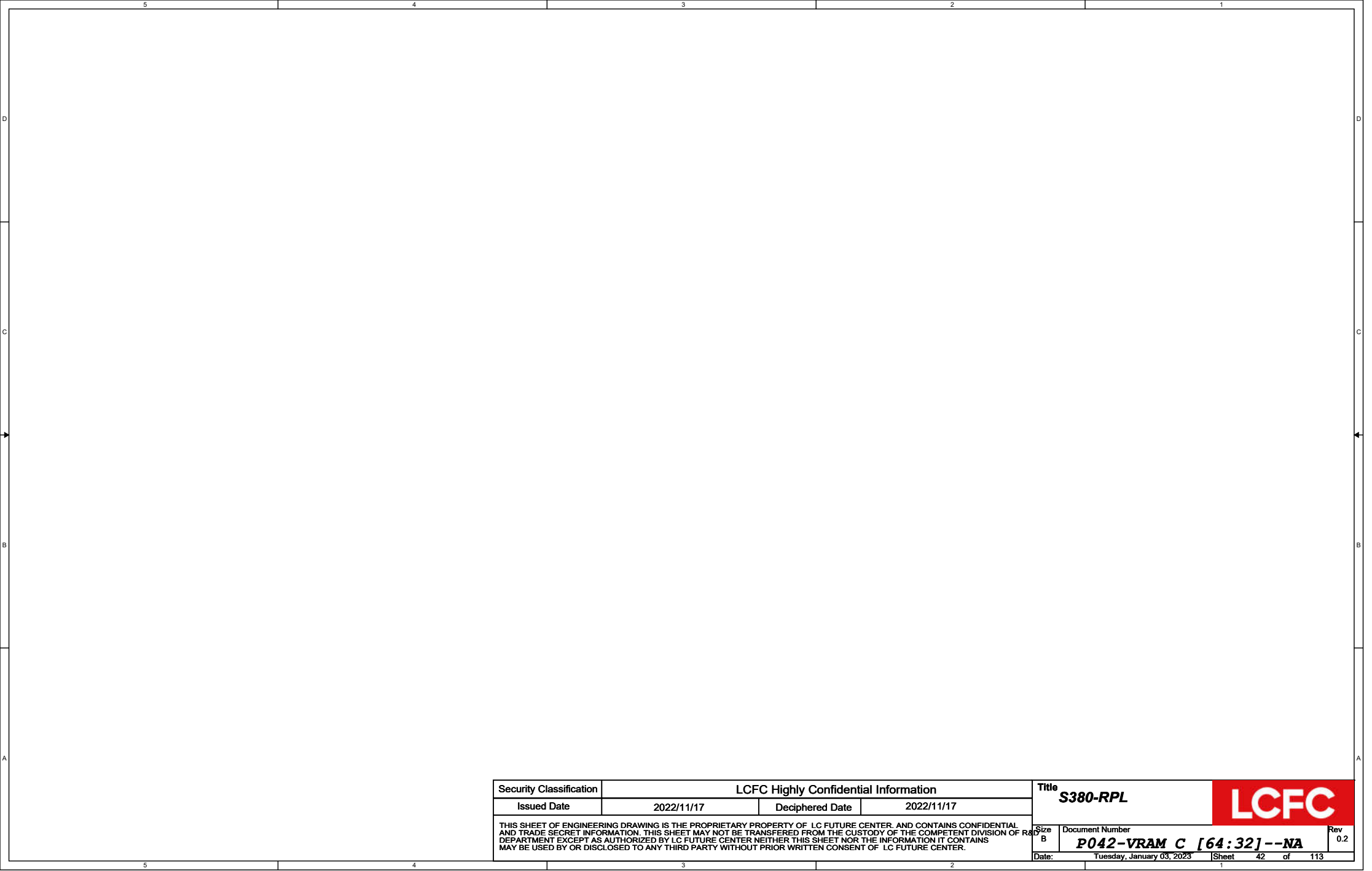
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				P039-VRAM B [31:0]--NA			
Date:				Tuesday, January 03, 2023	Sheet	39 of 113	

Change list:
Remove GPU Circuit

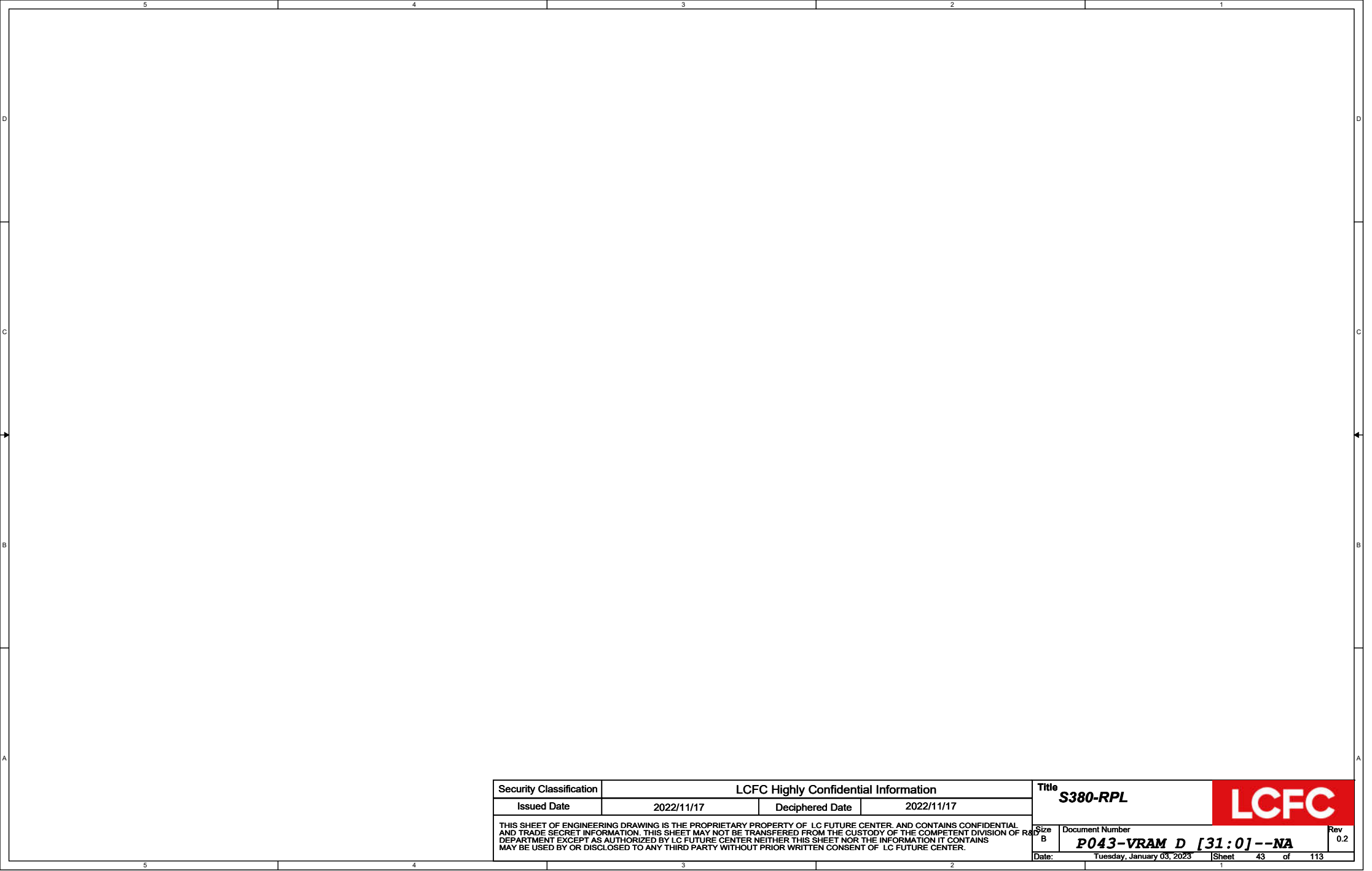
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						B	P040-VRAM B [64:32] --NA		0.2
						Date:	Tuesday, January 03, 2023		Sheet

Change list:
Remove GPU Circuit

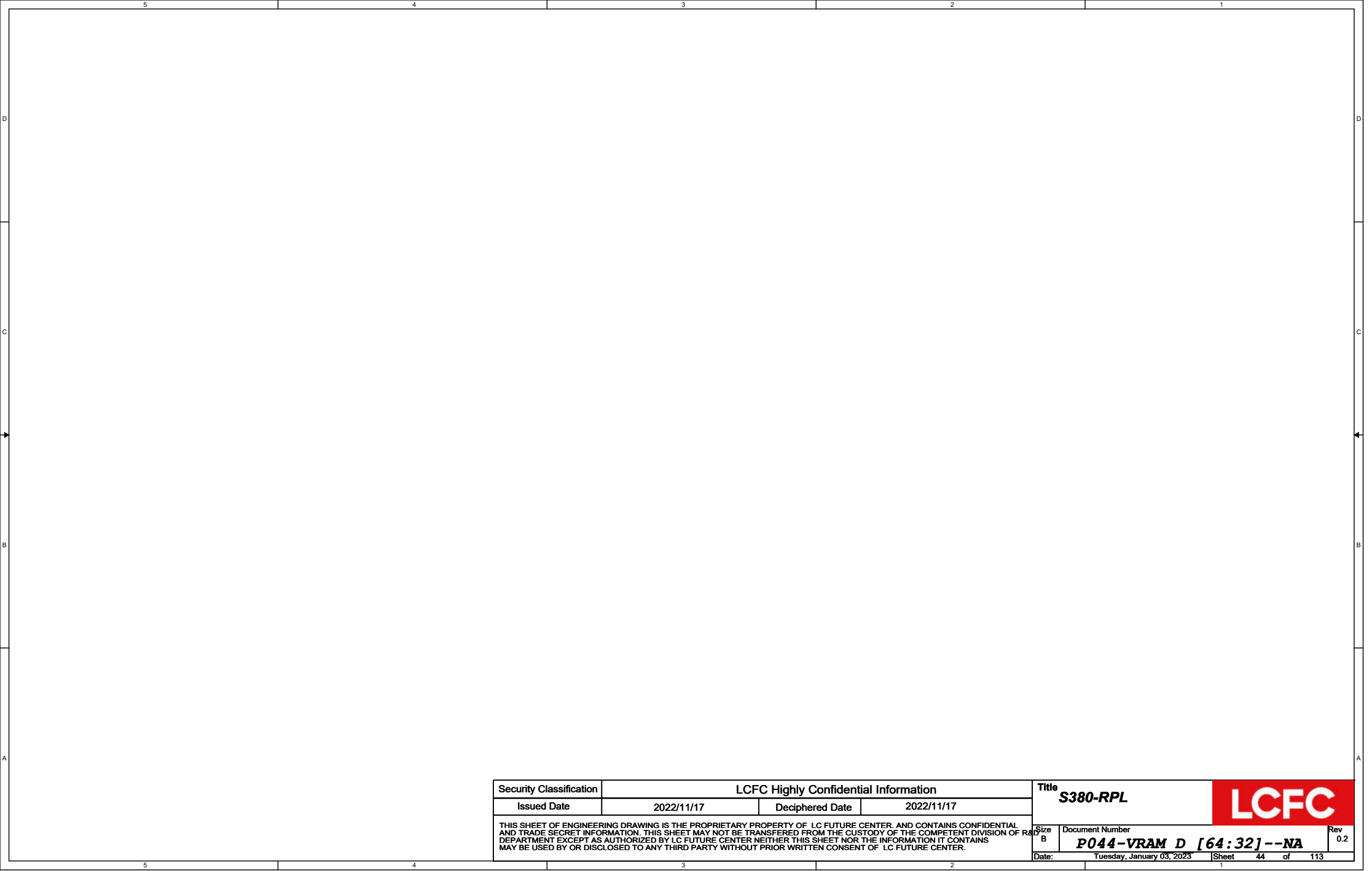
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				B	P042-VRAM C [64:32]--NA	0.2	
Date:				Tuesday, January 03, 2023	Sheet	42 of 113	



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					P043-VRAM D [31:0]--NA		
				Date:	Tuesday, January 03, 2023	Sheet 43 of 113	



D

C

B

A

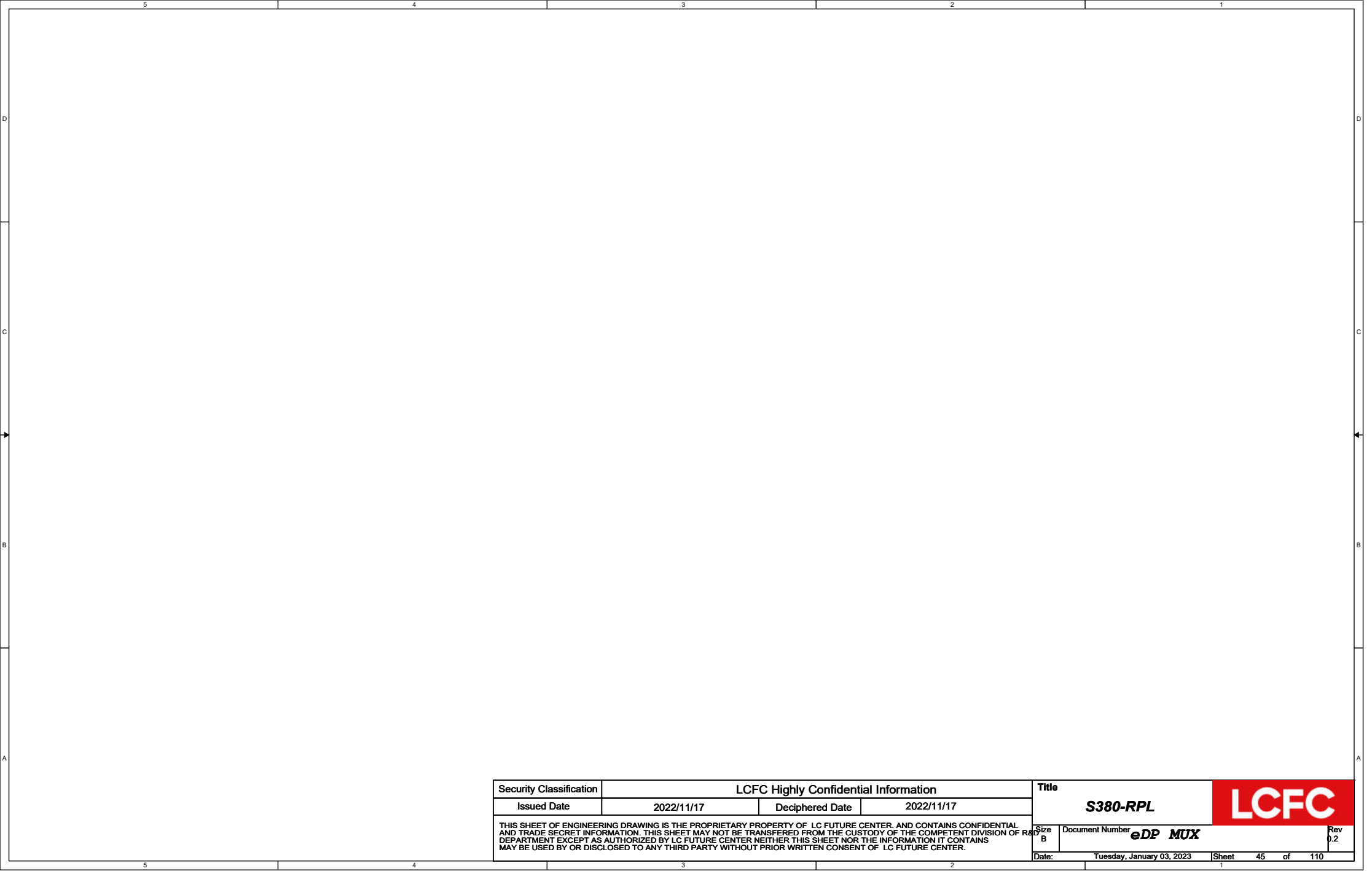
D

C

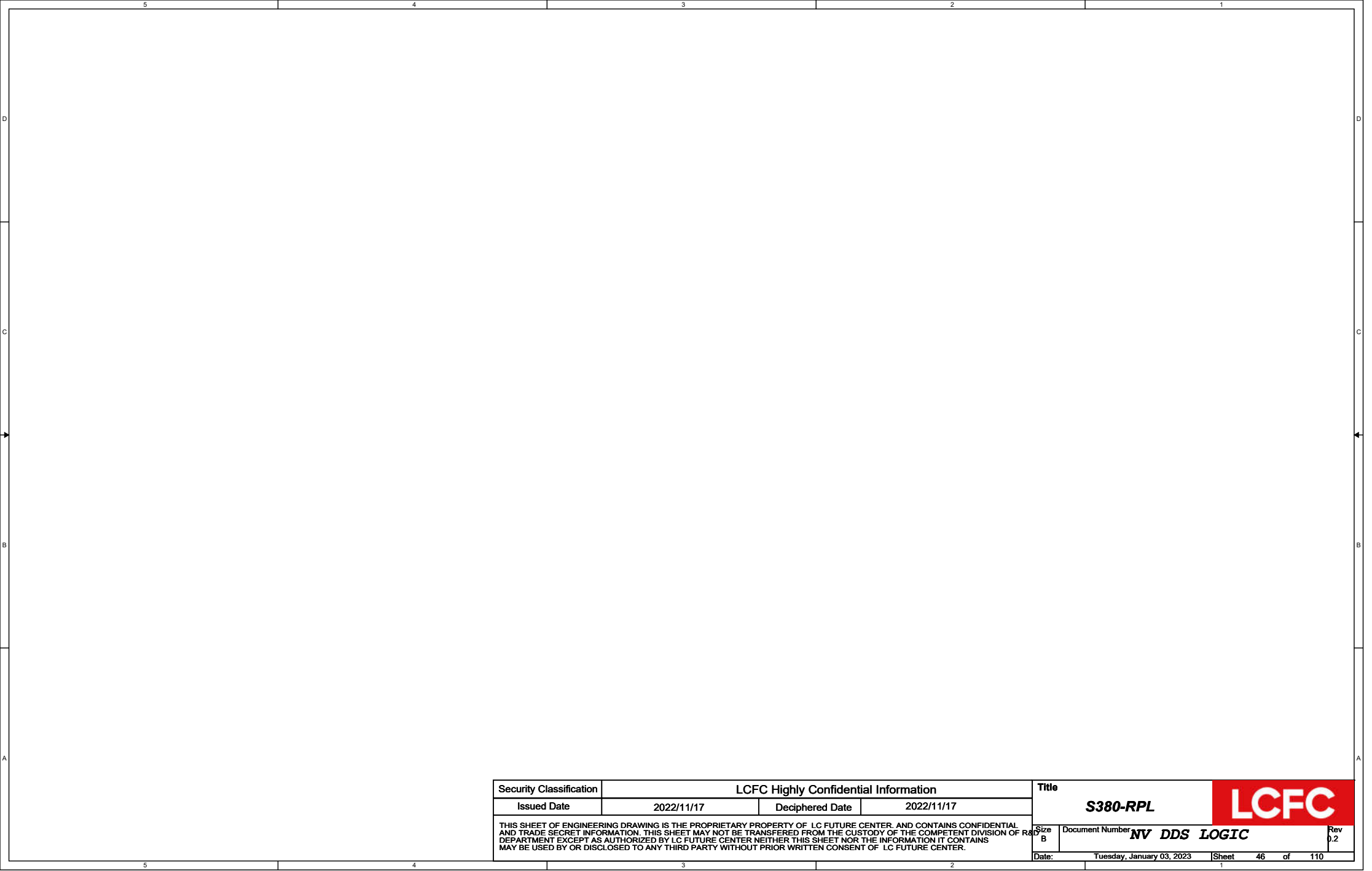
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A

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				Date:	Tuesday, January 03, 2023	Sheet 44 of 113	

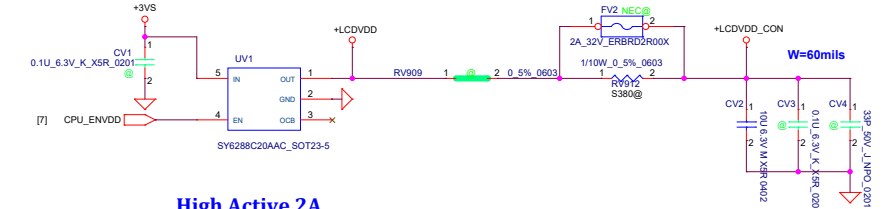


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				Date:	Tuesday, January 03, 2023	Sheet 45 of 110

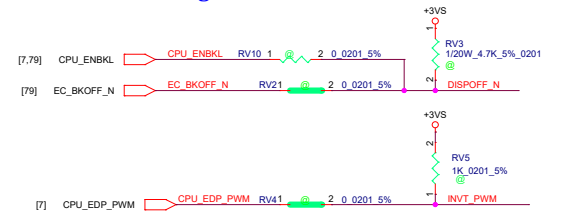


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					B	NV DDS LOGIC	0.2
					Date:	Tuesday, January 03, 2023	Sheet

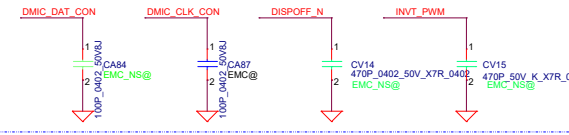
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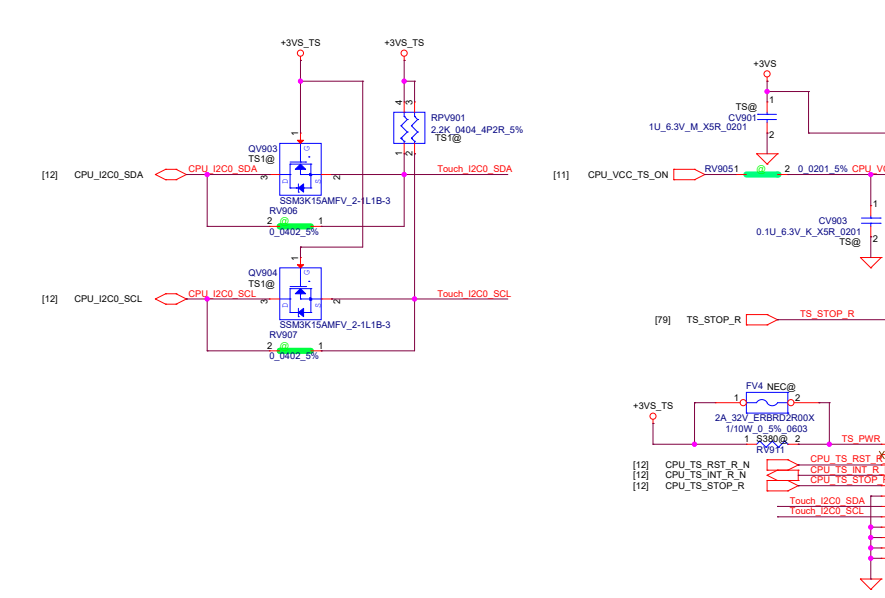
High Active 2A



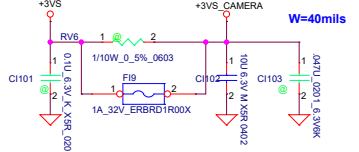
EMC close to connector



Touch Screen

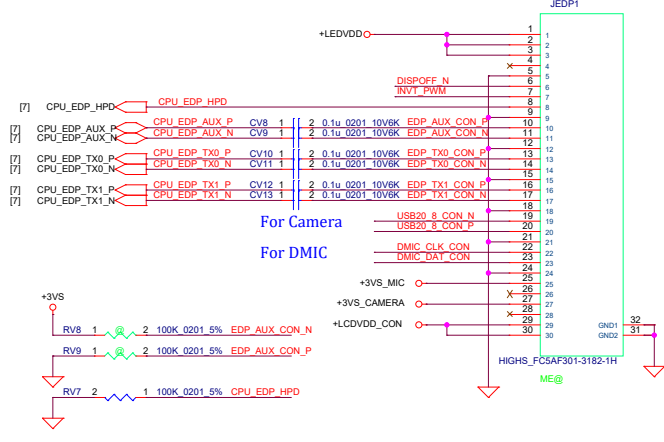


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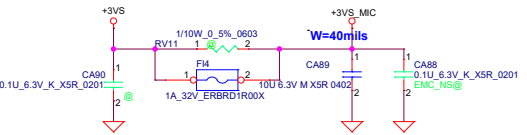


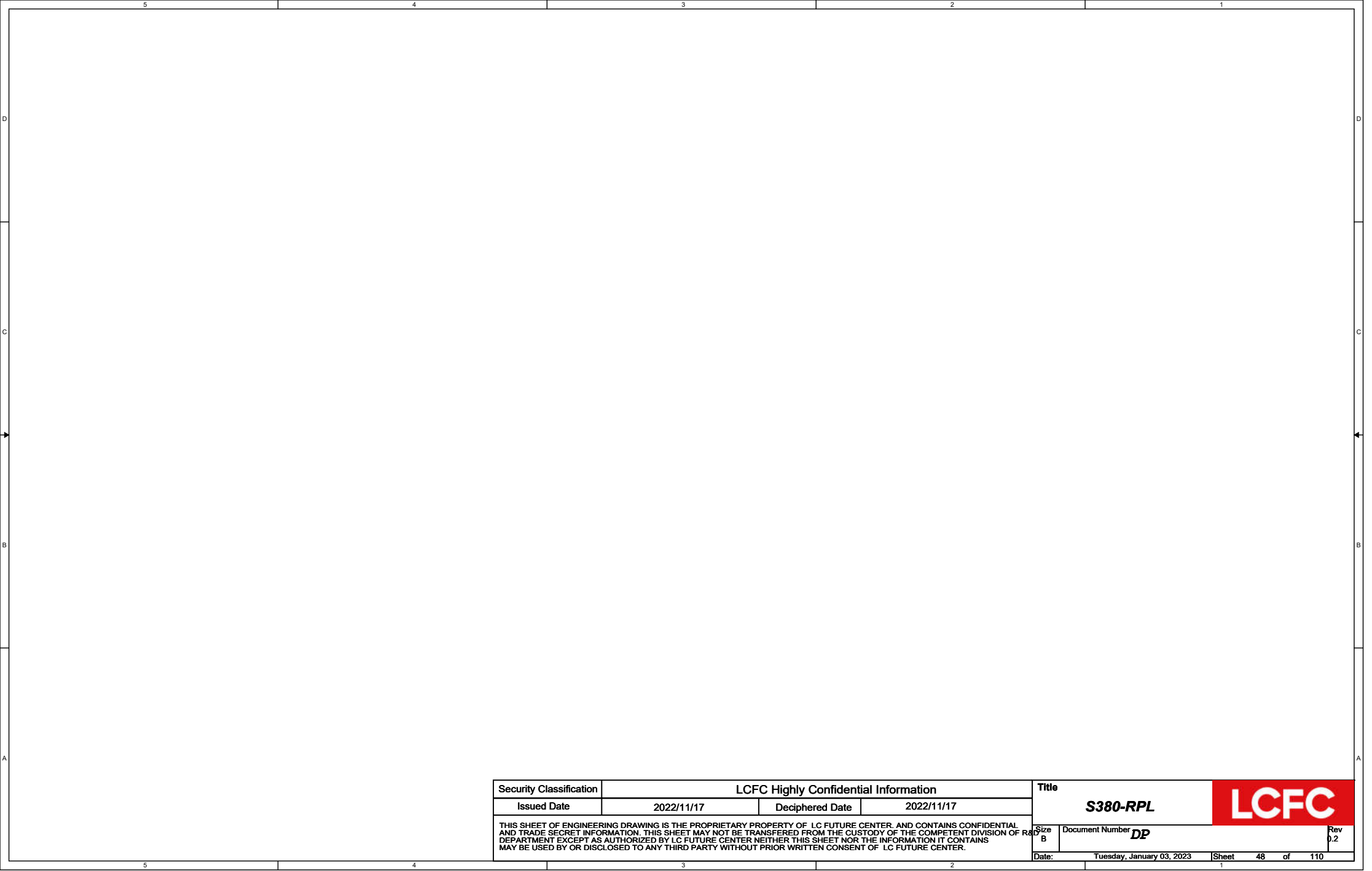
For Camera


For DMIC

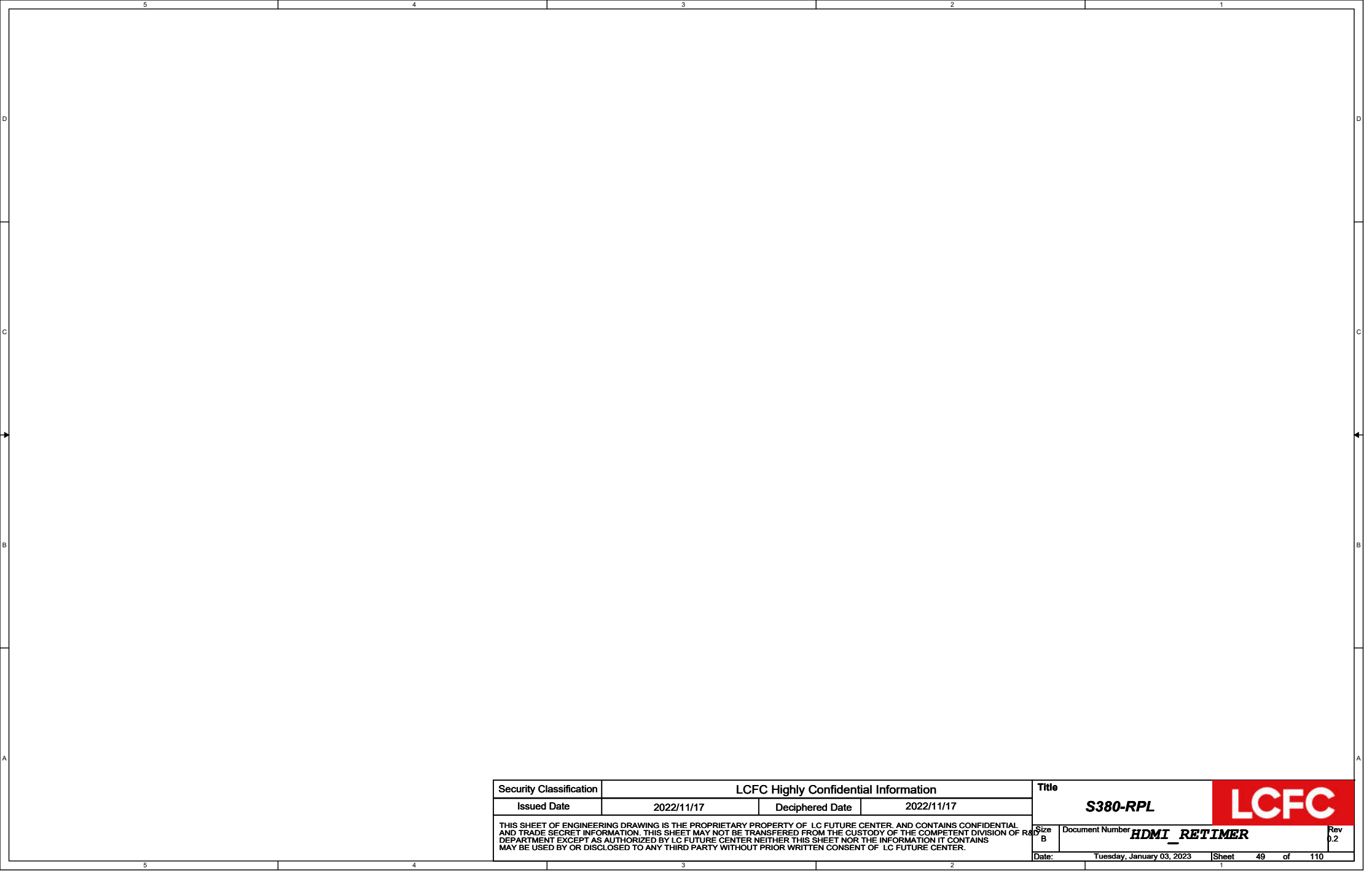


DMIC



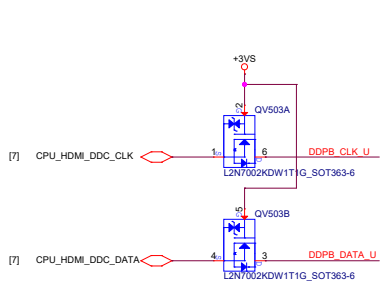
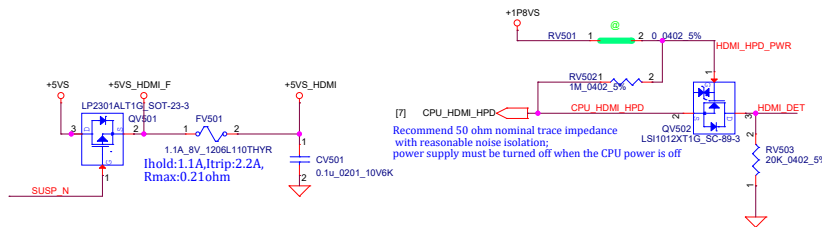


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				Date:	Tuesday, January 03, 2023	Sheet	48 of 110



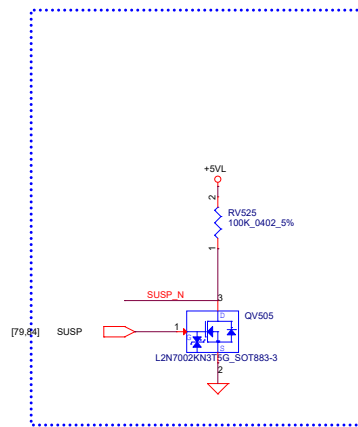
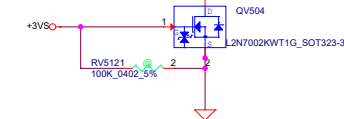
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				1 of 110		

HDMI Power

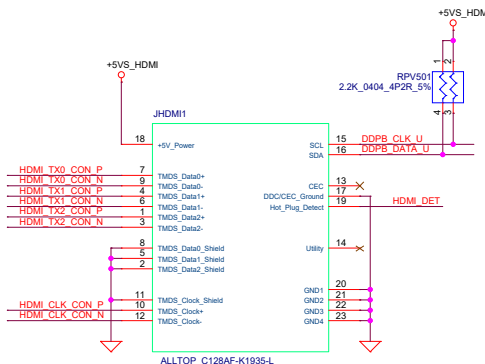
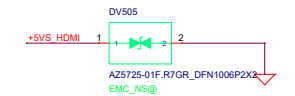
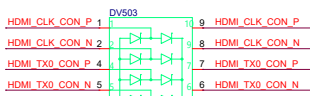
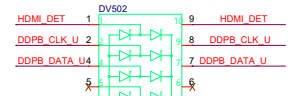
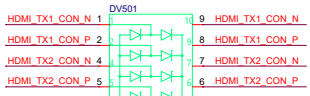
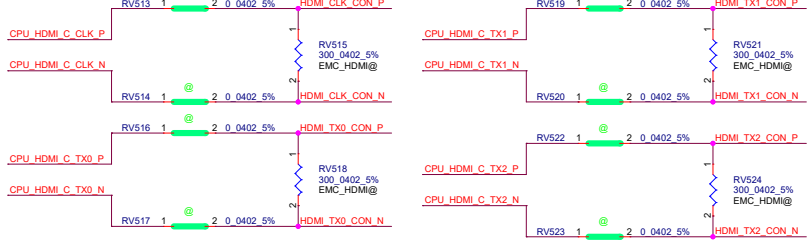


[7]	CPU_HDMI_TX0_P	CPU_HDMI_TX0_P	CV5021	2	0.1u	0201_10V6K	CPU_HDMI_C_TX0_P
[7]	CPU_HDMI_TX0_N	CPU_HDMI_TX0_N	CV5031	2	0.1u	0201_10V6K	CPU_HDMI_C_TX0_N
[7]	CPU_HDMI_TX1_P	CPU_HDMI_TX1_P	CV5041	2	0.1u	0201_10V6K	CPU_HDMI_C_TX1_P
[7]	CPU_HDMI_TX1_N	CPU_HDMI_TX1_N	CV5051	2	0.1u	0201_10V6K	CPU_HDMI_C_TX1_N
[7]	CPU_HDMI_TX2_P	CPU_HDMI_TX2_P	CV5061	2	0.1u	0201_10V6K	CPU_HDMI_C_TX2_P
[7]	CPU_HDMI_TX2_N	CPU_HDMI_TX2_N	CV5071	2	0.1u	0201_10V6K	CPU_HDMI_C_TX2_N
[7]	CPU_HDMI_CLK_P	CPU_HDMI_CLK_P	CV5081	2	0.1u	0201_10V6K	CPU_HDMI_C_CLK_P
[7]	CPU_HDMI_CLK_N	CPU_HDMI_CLK_N	CV5091	2	0.1u	0201_10V6K	CPU_HDMI_C_CLK_N

CPU_HDMI_C_TX0_P	RV5041	2	470	0402_5%	
CPU_HDMI_C_TX0_N	RV5051	2	470	0402_5%	
CPU_HDMI_C_TX1_P	RV5061	2	470	0402_5%	
CPU_HDMI_C_TX1_N	RV5071	2	470	0402_5%	
CPU_HDMI_C_TX2_P	RV5081	2	470	0402_5%	
CPU_HDMI_C_TX2_N	RV5091	2	470	0402_5%	
CPU_HDMI_C_CLK_P	RV5101	2	470	0402_5%	
CPU_HDMI_C_CLK_N	RV5111	2	470	0402_5%	



EMC



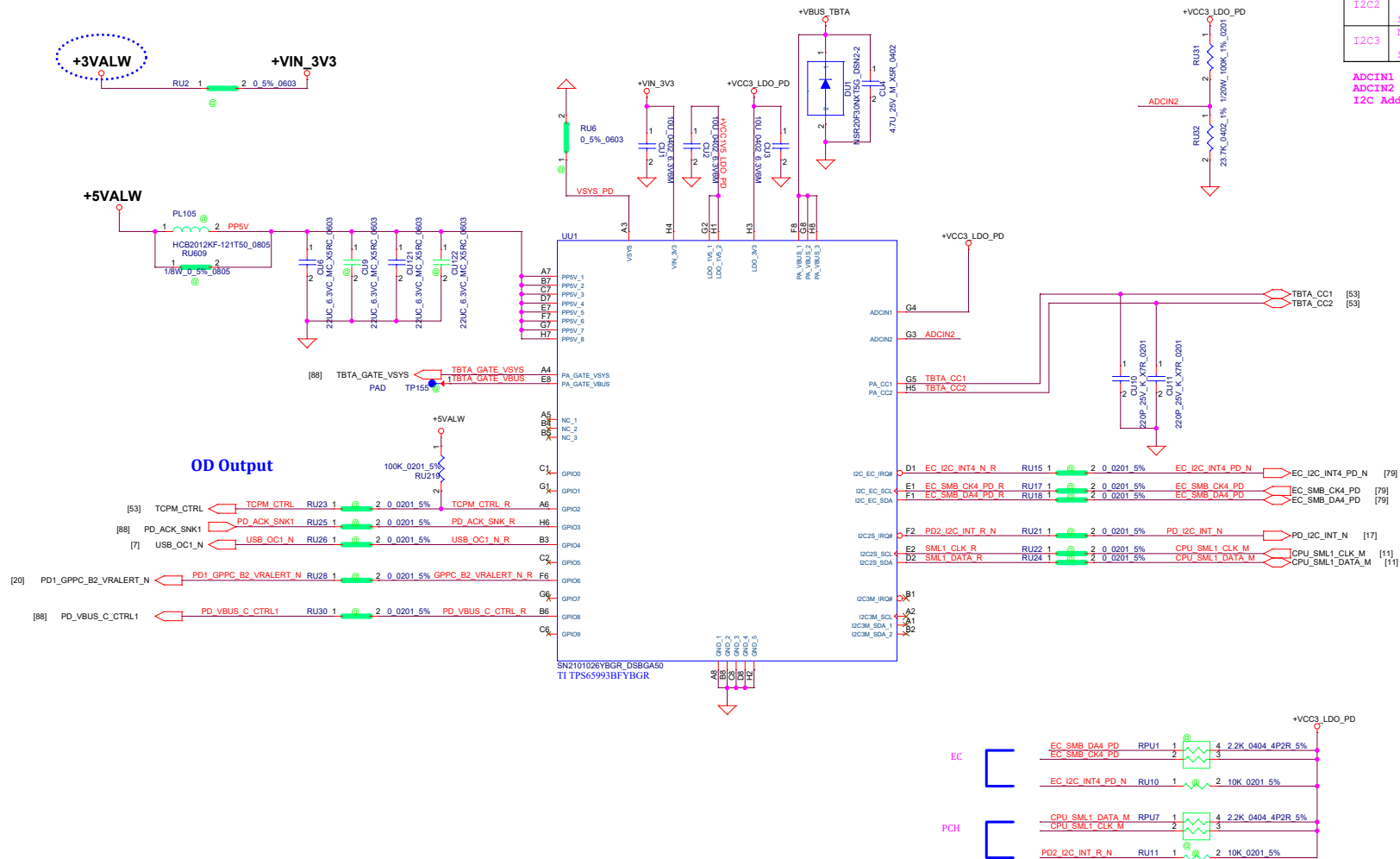


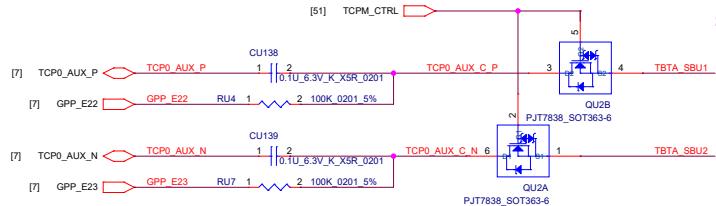
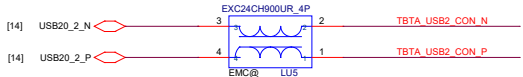
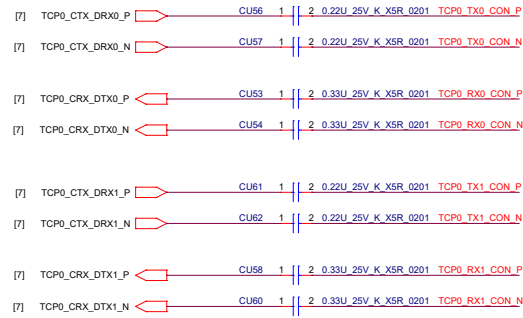
TABLE I2C Addressing

I2C1	Master: EC	TBTA PORT	0x20
I2C2	Master: PMC	TBTA PORT	0x20
I2C3	Master: PD	TBTA PORT	0x20
	Slave: PD	TBTA PORT	0x20
	Slave: RT	TBTA PORT	0x20

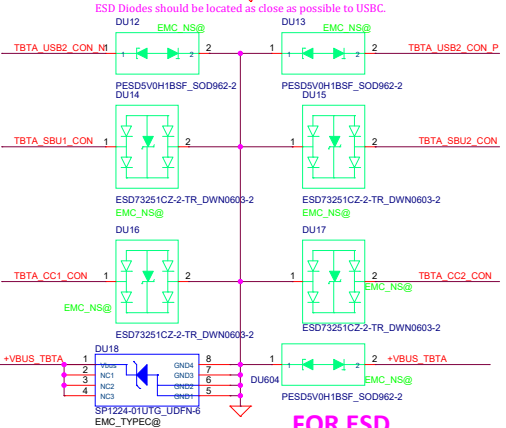
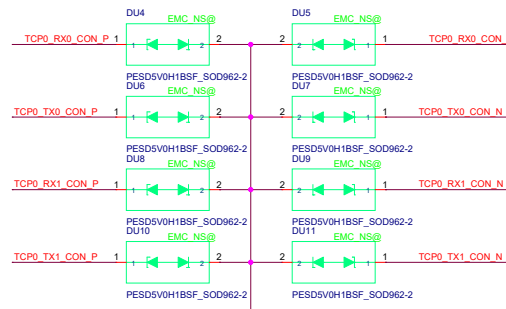
ADCIN1 Decoded:7 --tie to LDO_3V3
ADCIN2 Decoded:3 --0.1916
I2C Address Index: 1#

5	4	3	2	1
D				D
C				C
B				B
A				A

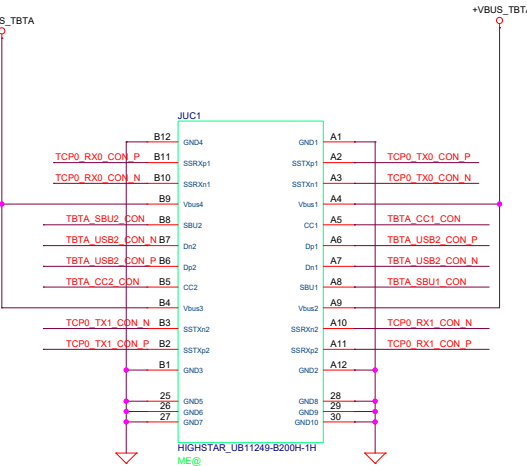
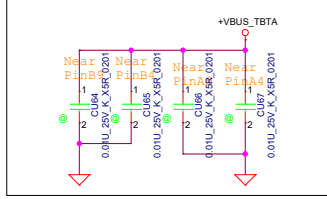
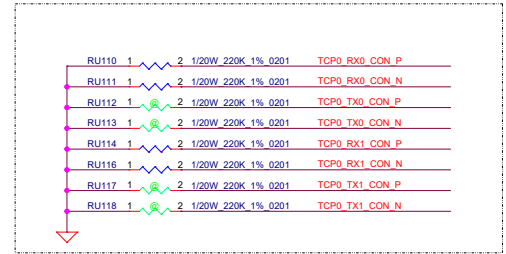
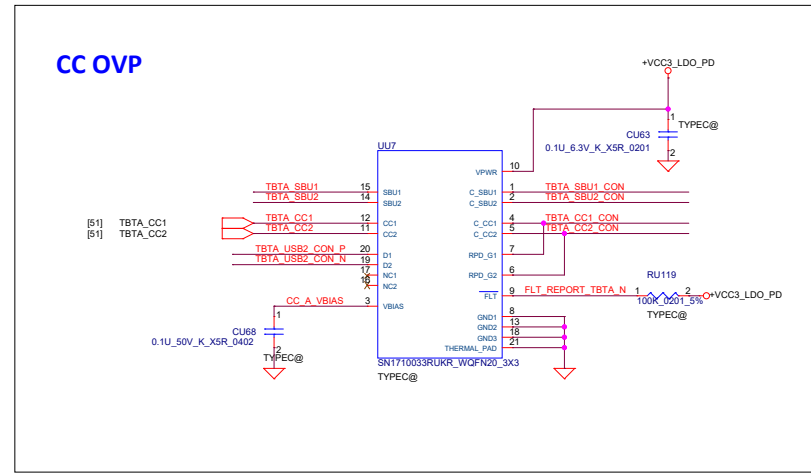
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Sideband signals for use by alternate:
DP mode - AUX signals
USB 4 mode - LSx signals

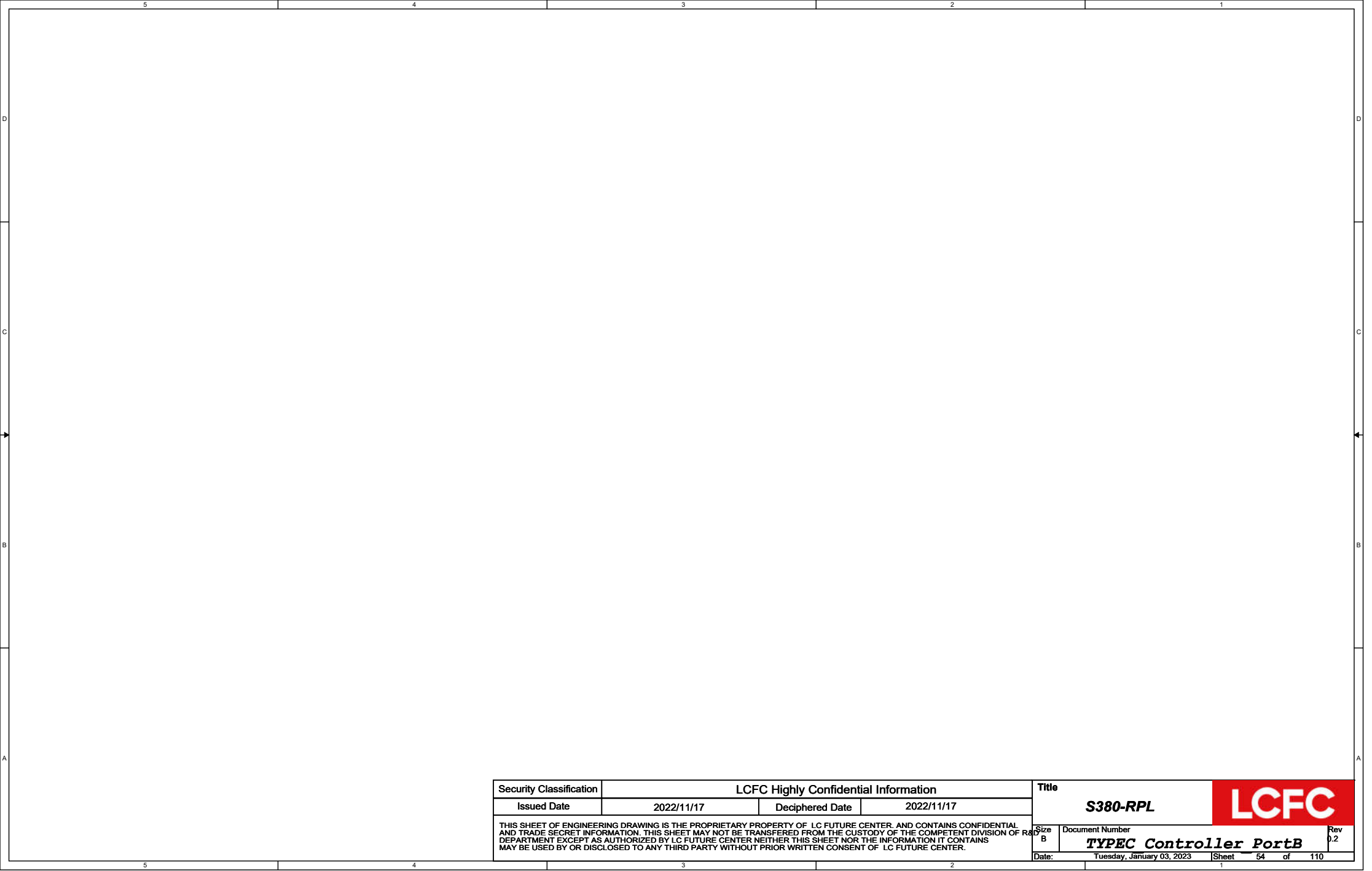


FOR ESD

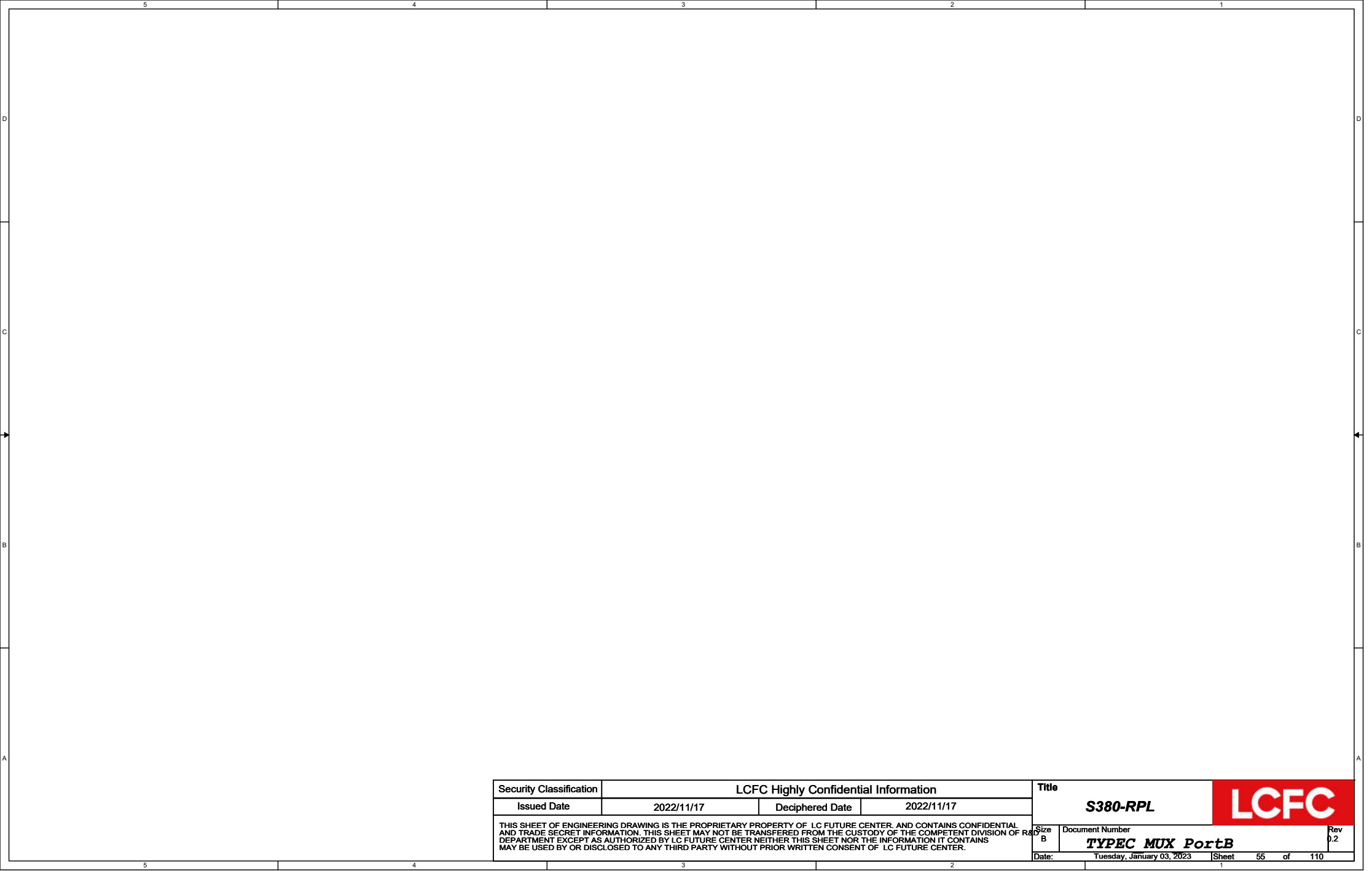


0425 Connector list Use SP060008900 UB11249-B200H-1H

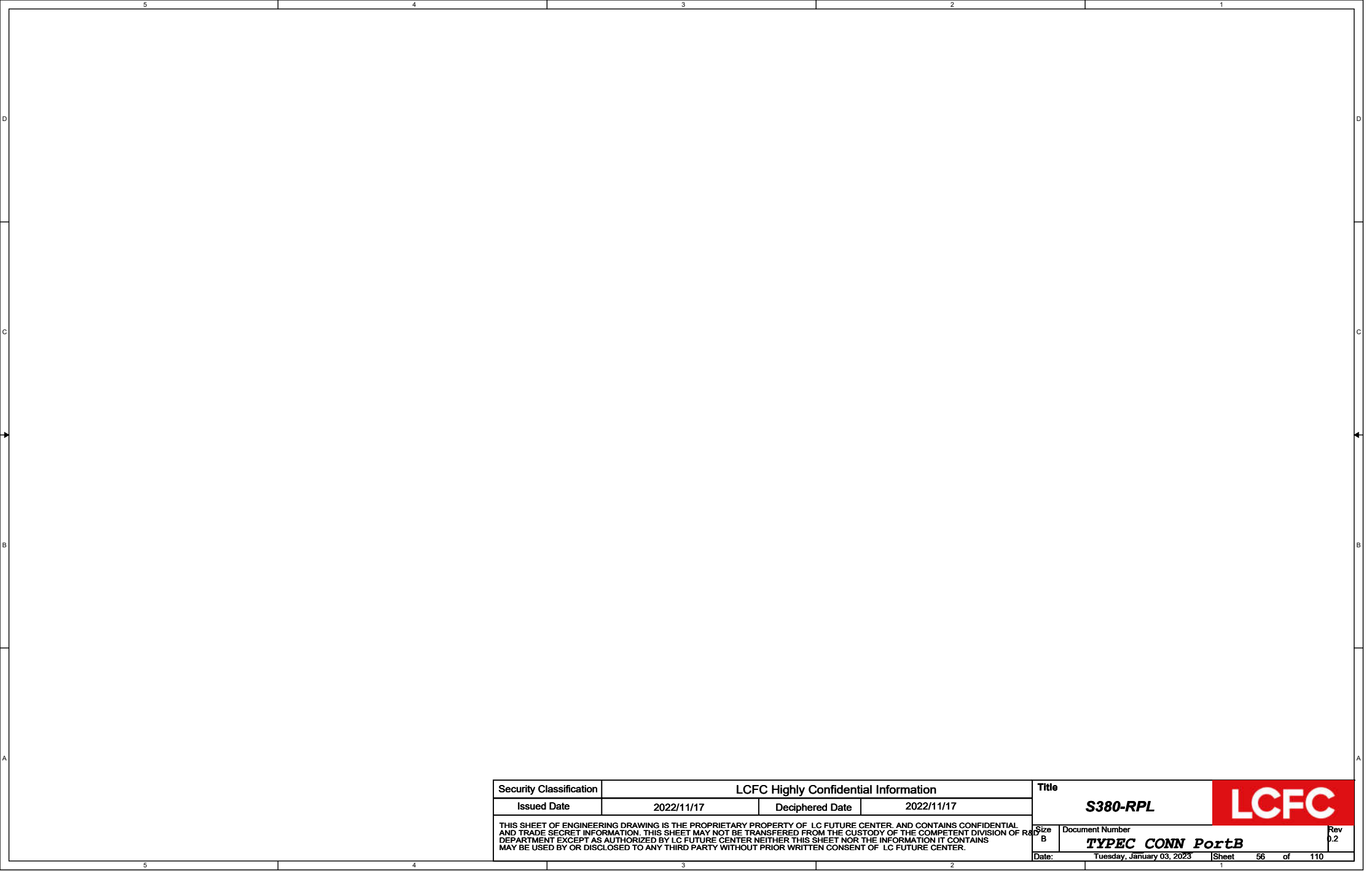
1124x
5=5" gold plating
9=30" gold plating
B200H
W=鍍黑鎳
H=鍍白鎳



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				Date: Tuesday, January 03, 2023	Sheet 54 of 110	Rev 0.2

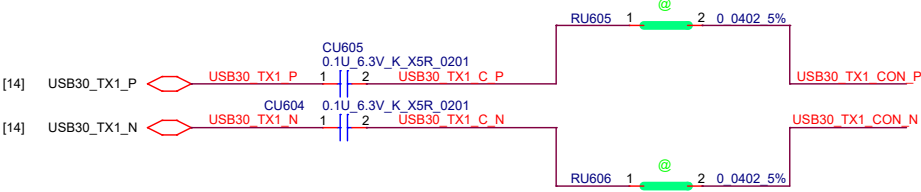
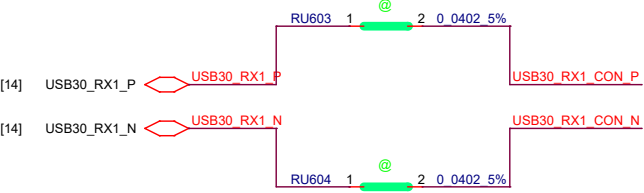
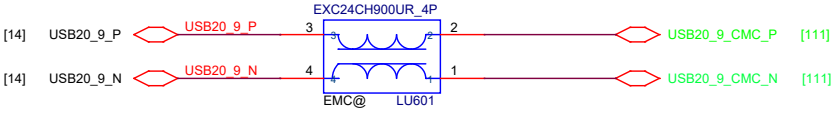
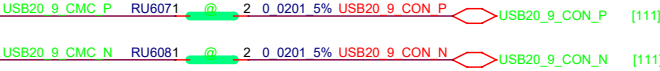
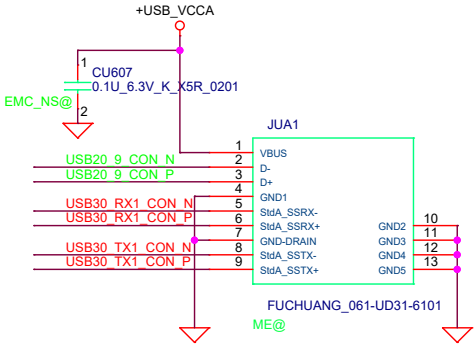
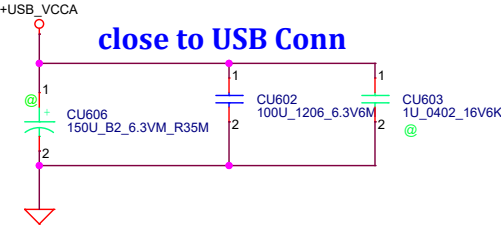
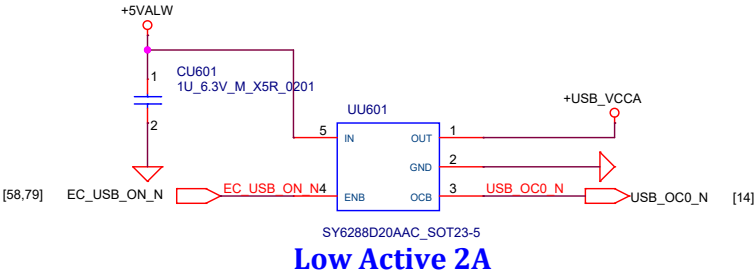


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				Date: Tuesday, January 03, 2023		Sheet 55 of 110

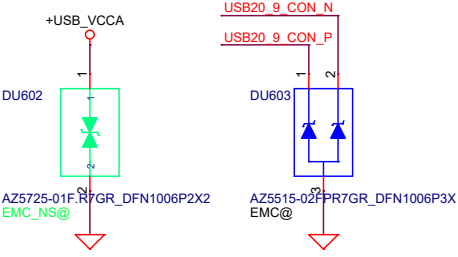
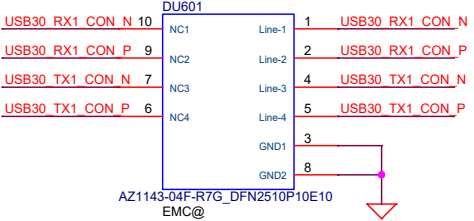


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				Date: Tuesday, January 03, 2023	Sheet 56 of 110	Rev 0.2

USB3.0 PORT



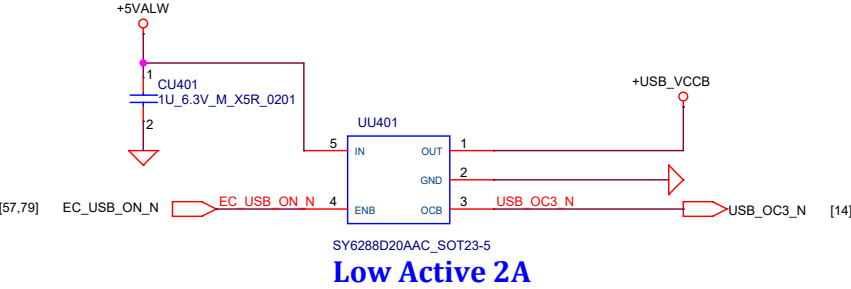
EMC close to USB Conn




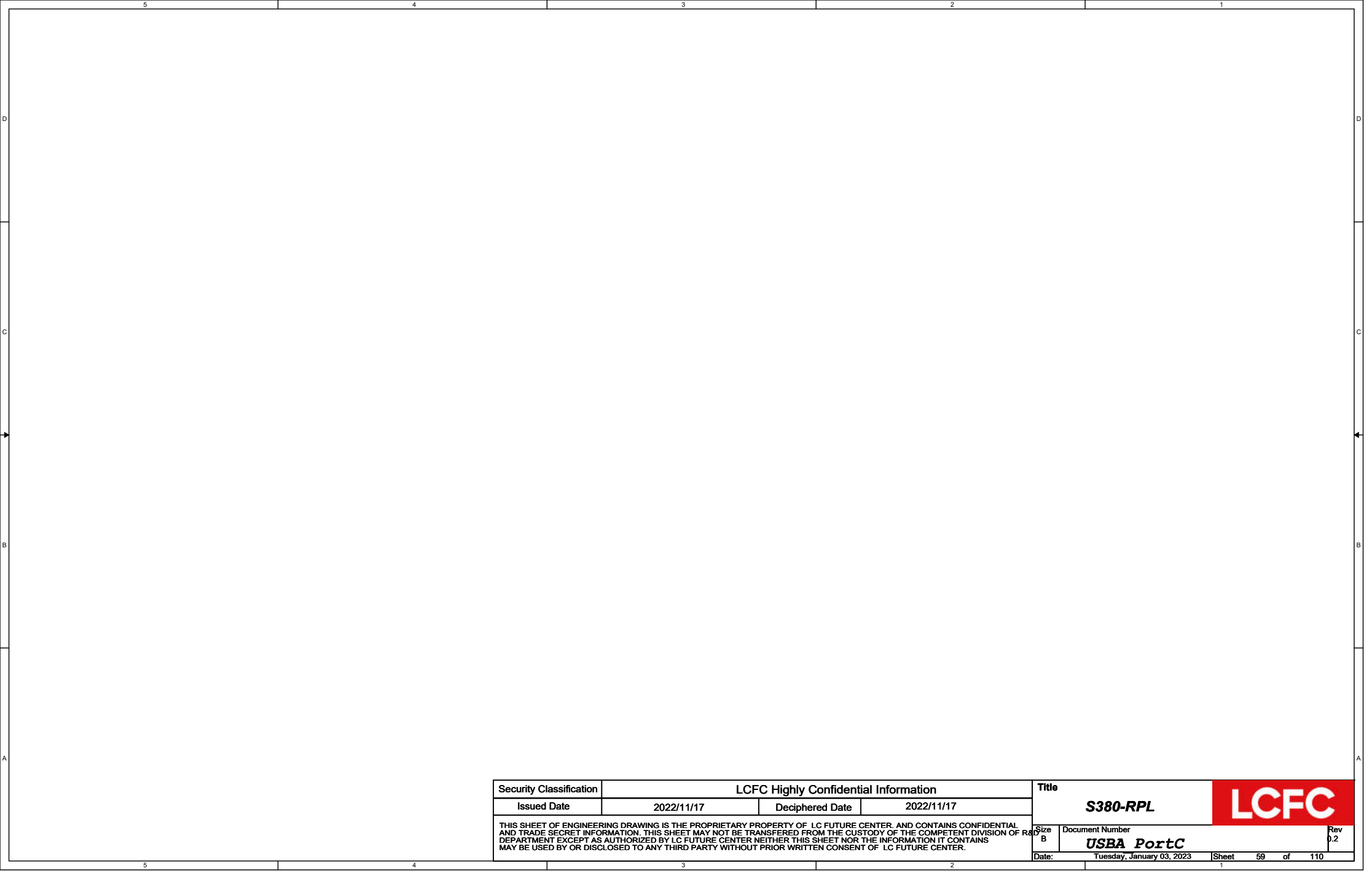
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Date:		Tuesday, January 03, 2023		Sheet		57		of		110			


USB3.0 Port and CMC&TVS&CAP MOVE to SUB Board

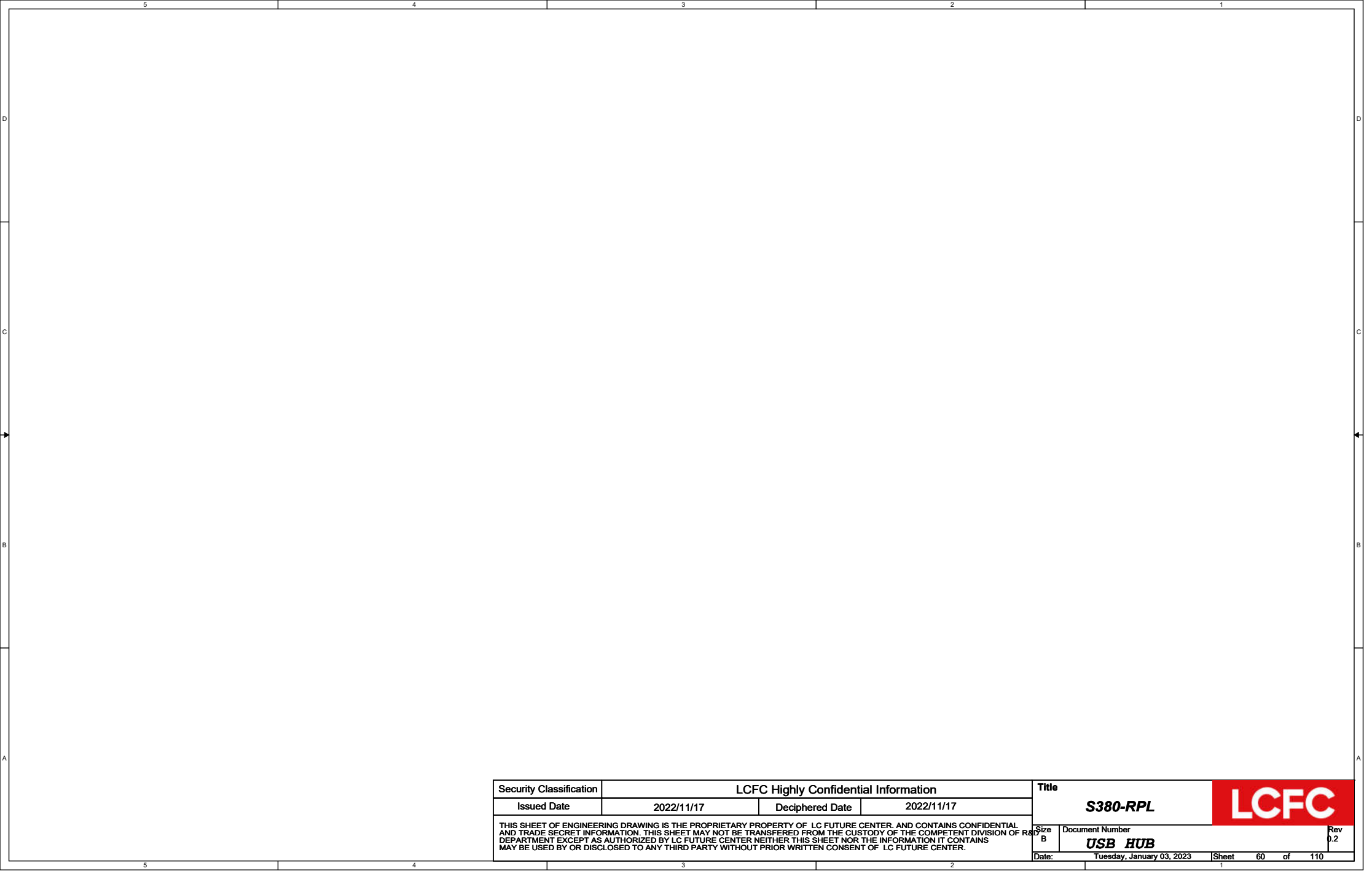
USB3.0 PORT




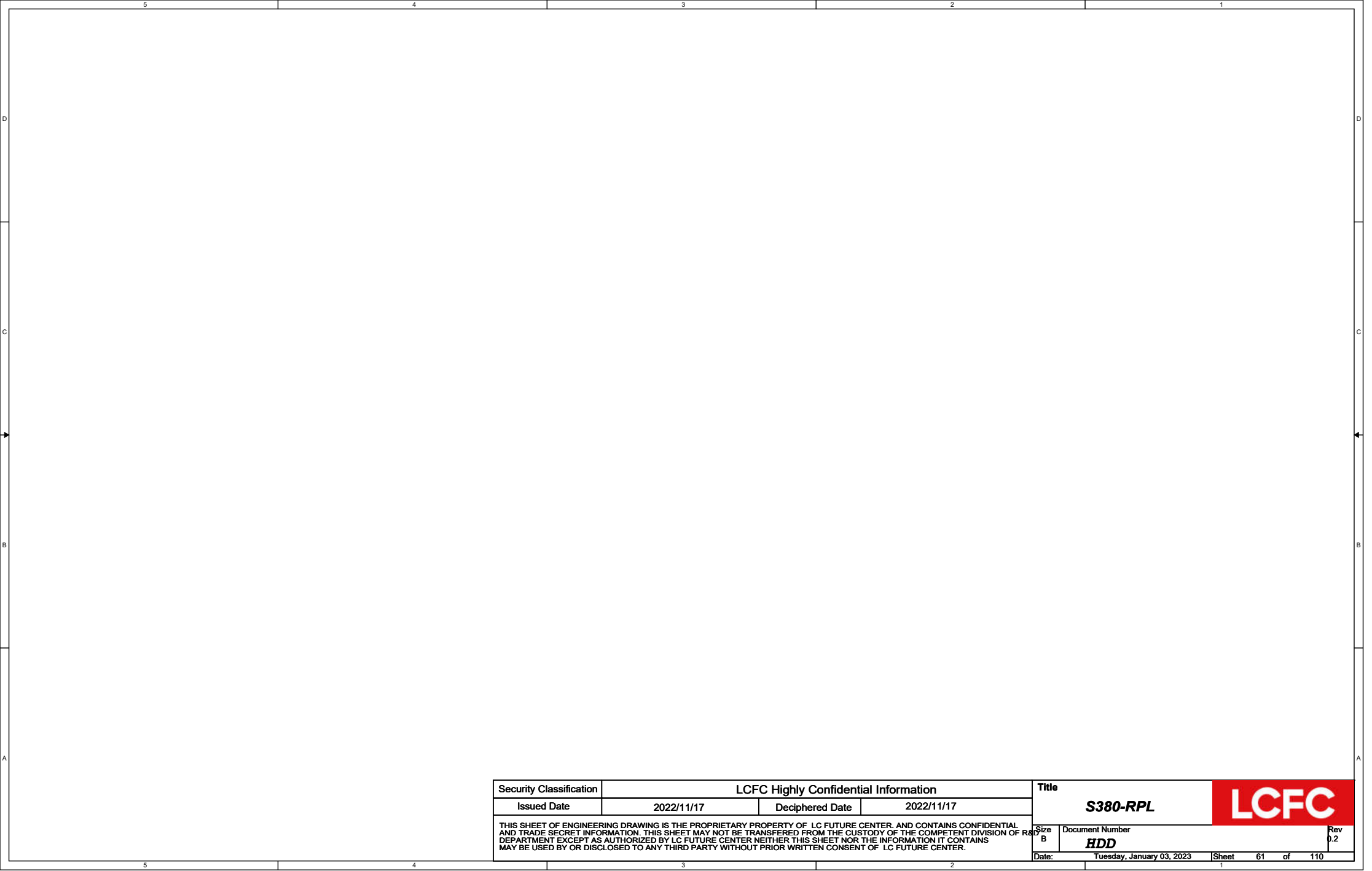
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				USBA PortB			
				Date:	Tuesday, January 03, 2023	Sheet 58 of 110	



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				Date: Tuesday, January 03, 2023		Sheet 59 of 110



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				B	USB HUB	0.2
				Date:	Tuesday, January 03, 2023	Sheet 60 of 110



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C


C

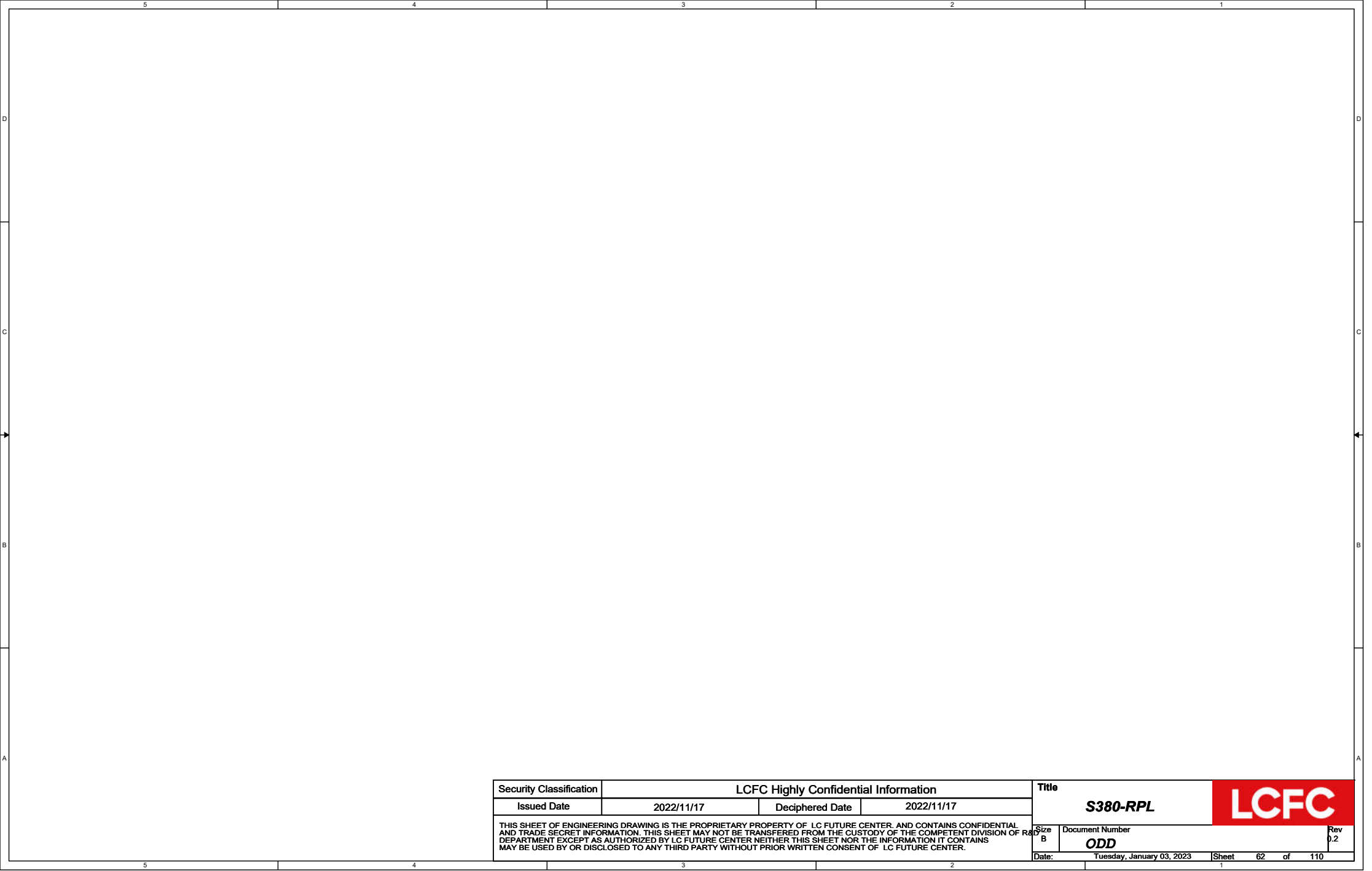
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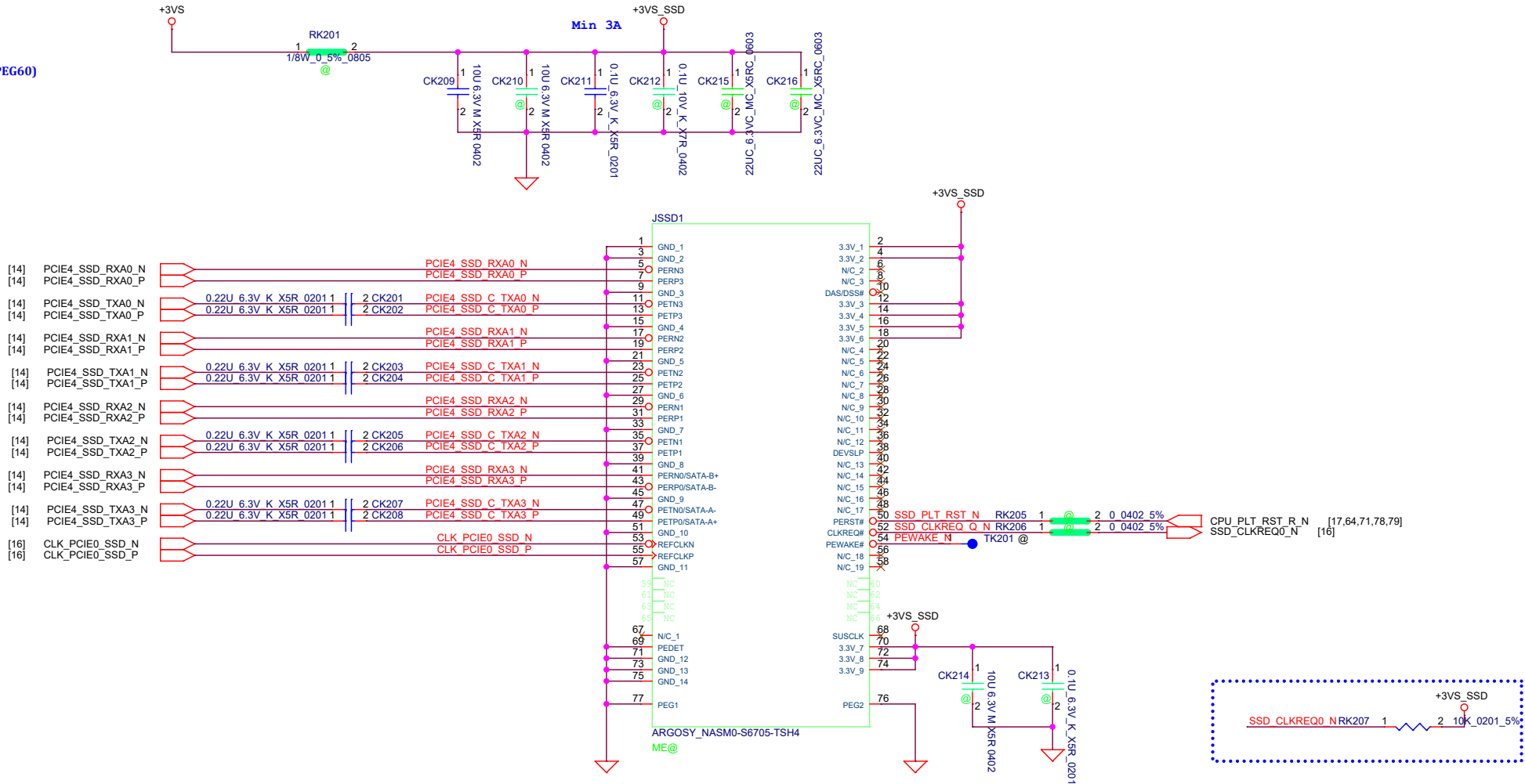
Security Classification	LCFC Highly Confidential Information				Title		
Issued Date	2022/11/17	Deciphered Date	2022/11/17	S380-RPL			
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				Date:	Tuesday, January 03, 2023	Sheet 61 of 110	



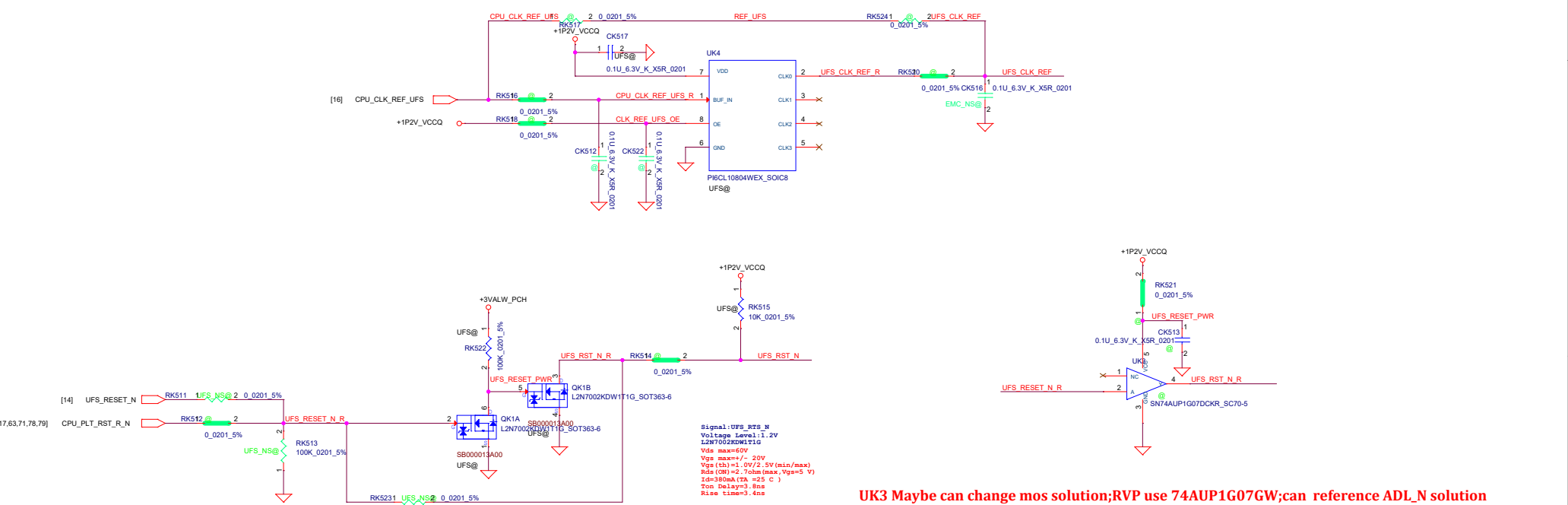
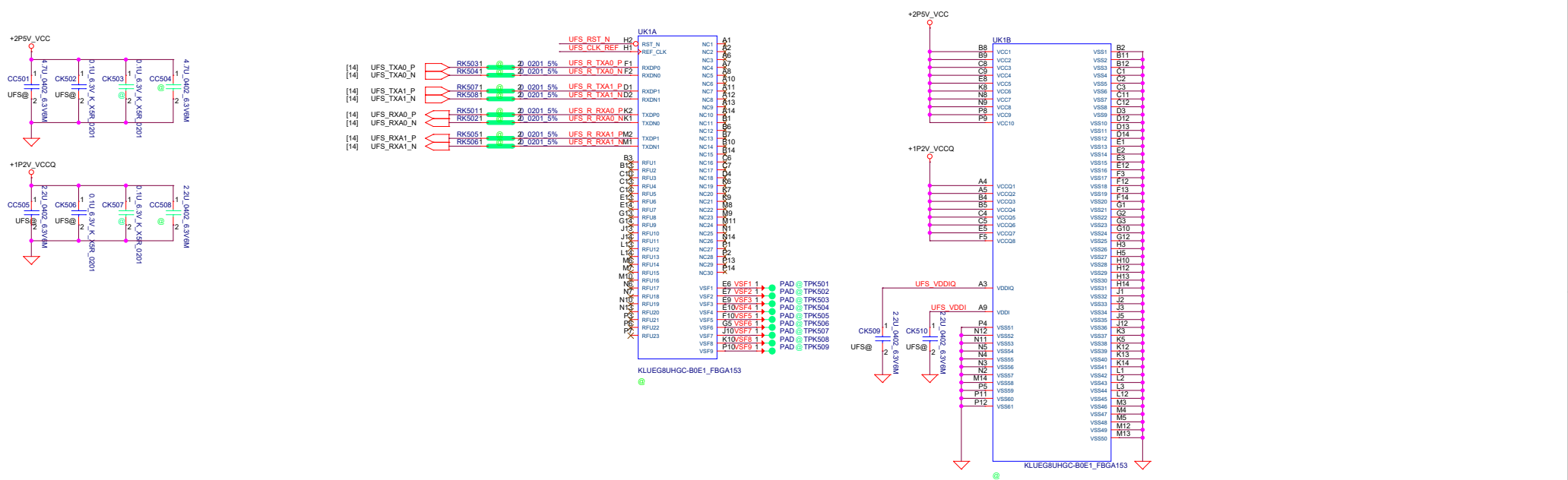
Security Classification	LCFC Highly Confidential Information			Title		
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				Date:	Tuesday, January 03, 2023	Sheet 62 of 110

SSD

PCIEX4_A (PEG60)

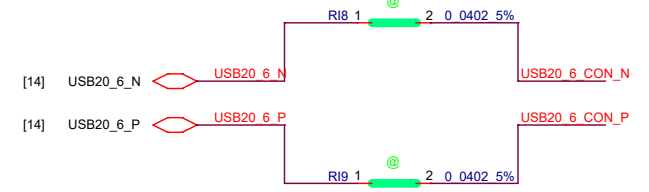
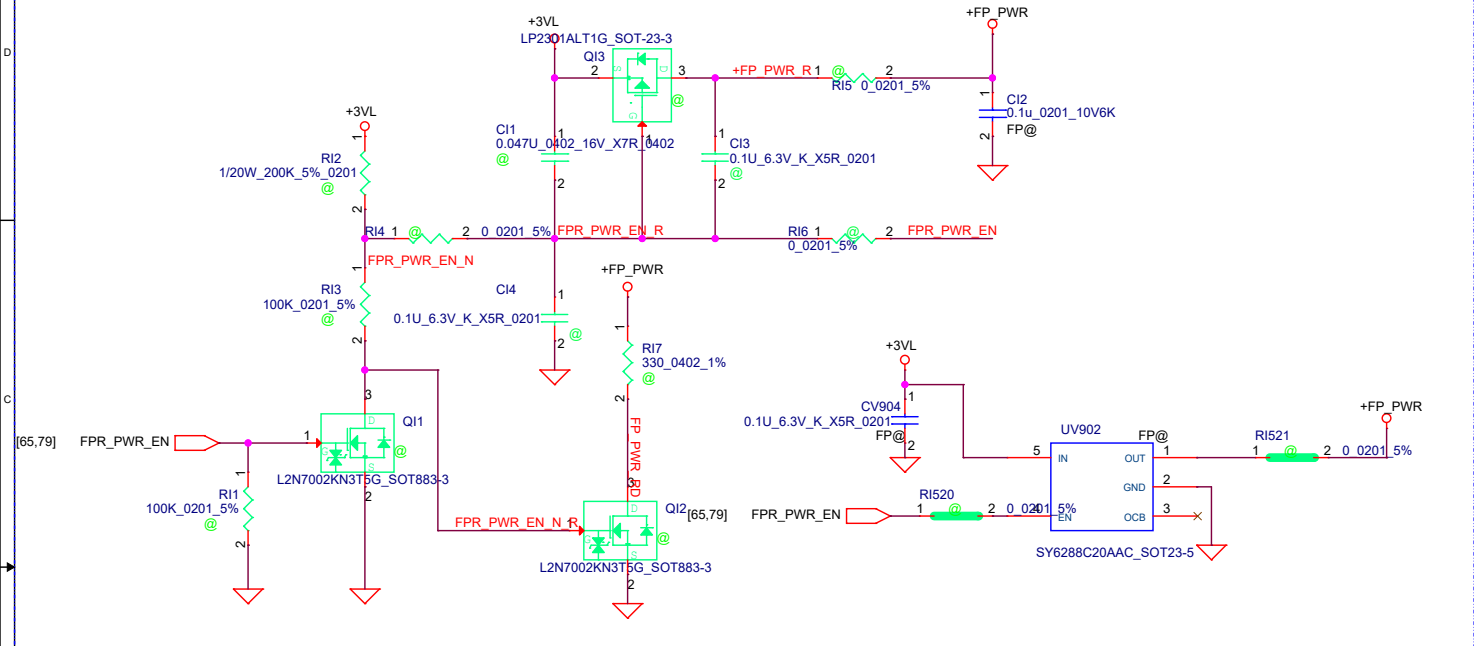


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Size		Document Number								Rev	
B		SSD								D.2	
Date:		Tuesday, January 03, 2023						Sheet		63 of 110	

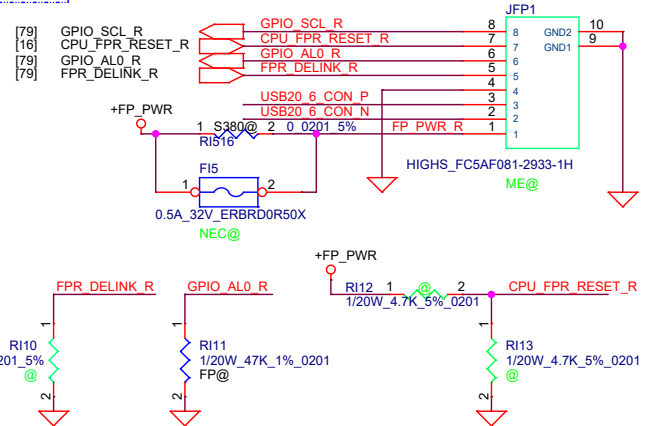
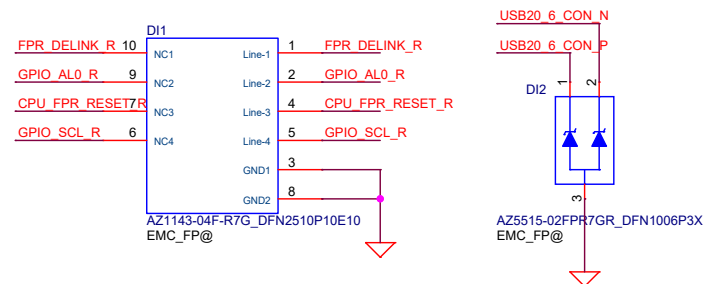


UK3 Maybe can change mos solution;RVP use 74AUP1G07GW;can reference ADL_N solution

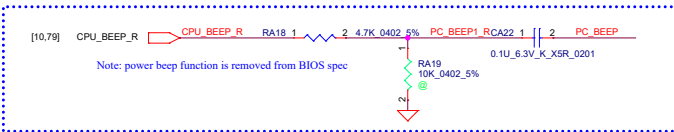
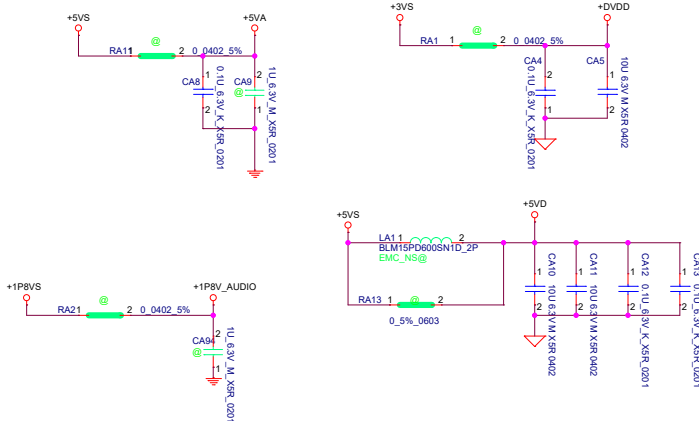
FP Power Control



EMC close to Conn



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		FPR								
Date:		Tuesday, January 03, 2023				Sheet		65 of 110		

[illegible]

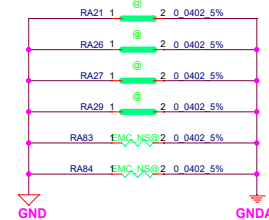
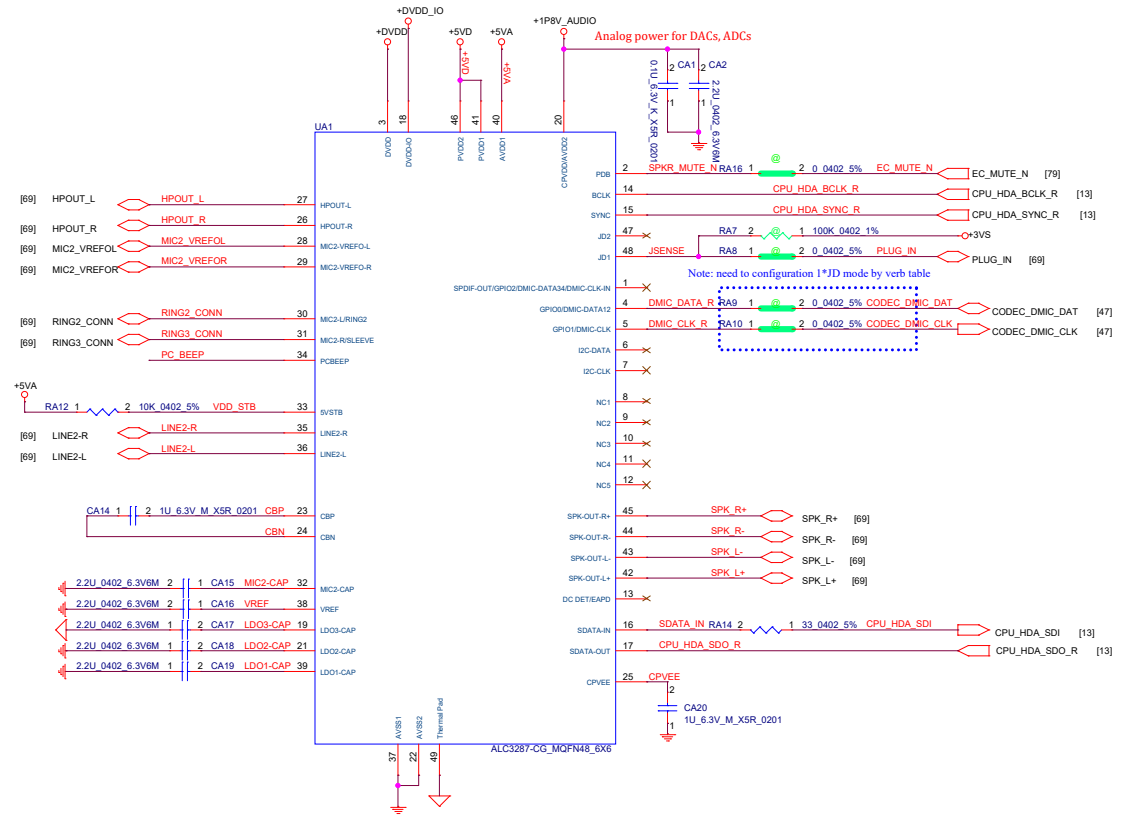
The diagram illustrates the pin connections for the CPU and CODEC. The left side shows the CPU connections, and the right side shows the CODEC connections. Each connection is represented by a pin number and a component value.


CPU Connections:

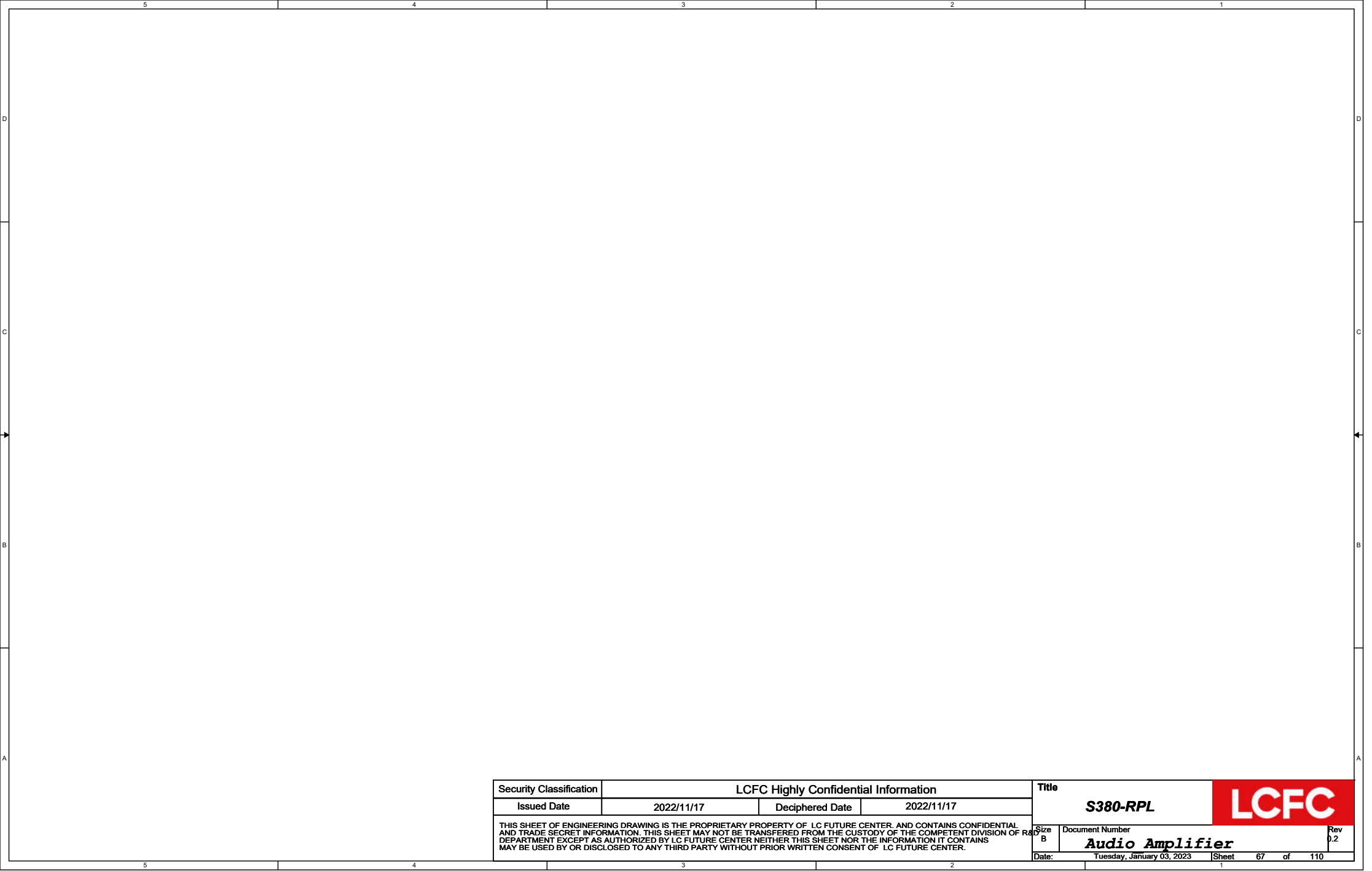
- CPU HDA_SYNC_R: Pin 1, 220K, ENL NSG
- CPU HDA_SDO_R: Pin 1, 220K, ENL NSG
- CPU HDA_BCLK_R: Pin 1, 220K, ENL NSG
- CPU HDA_SDI: Pin 1, 220K, ENL NSG
- HDA_BITCLK_AUDIO_R: Pin 1, 220K, ENL NSG
- HDA_SDO_R: Pin 1, 220K, ENL NSG

CODEC Connections:

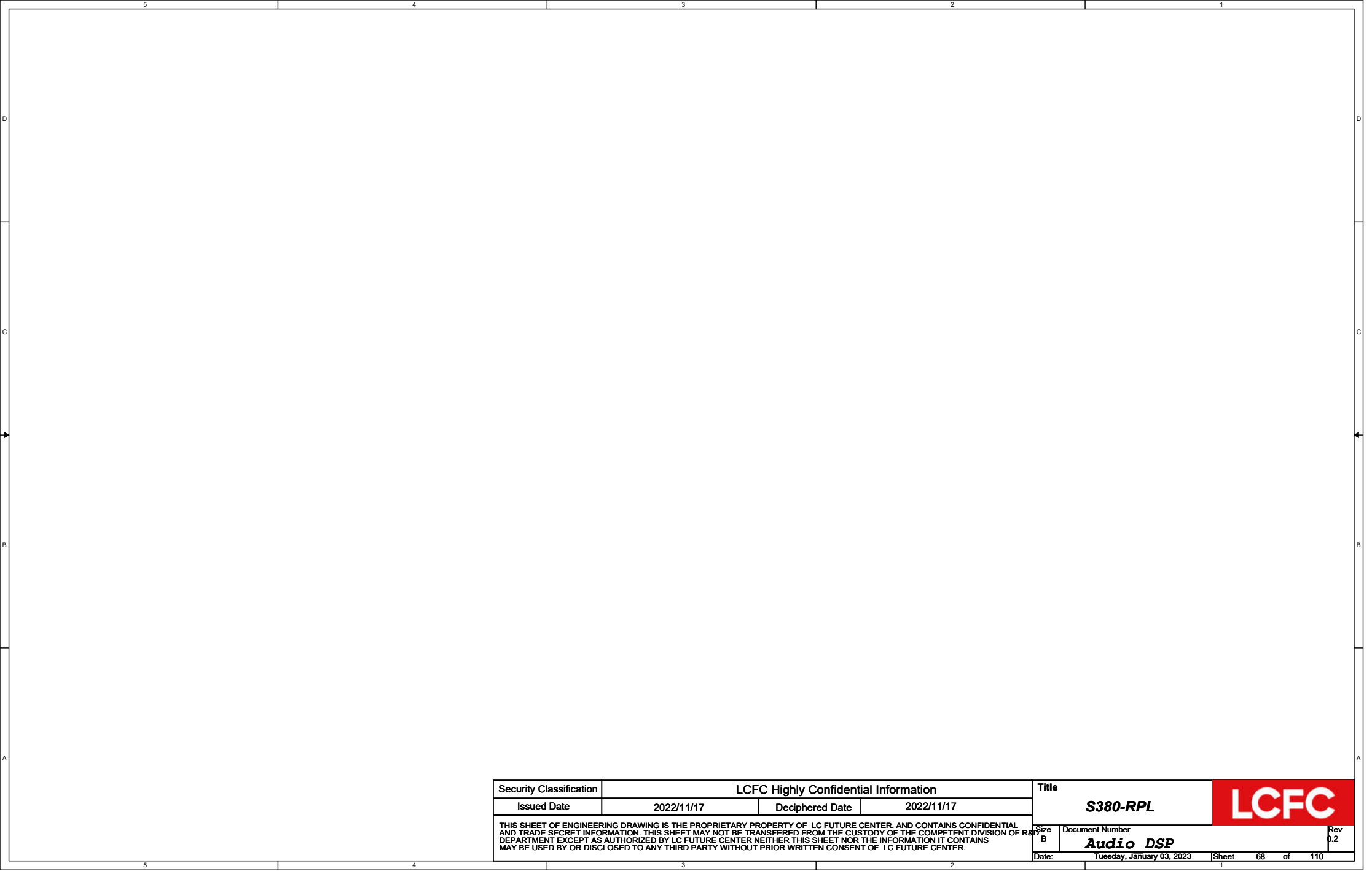
- CODEC DMIC_CLK: Pin 1, 220K, ENL NSG
- CODEC DMIC_DAT: Pin 1, 220K, ENL NSG
- HPOUT_L: Pin 1, 220K, ENL NSG
- HPOUT_R: Pin 1, 220K, ENL NSG




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Size C		Document Number						Rev		
		Audio Codec						0.2		
Date:		Tuesday, January 03, 2023				Sheet		66 of 110		

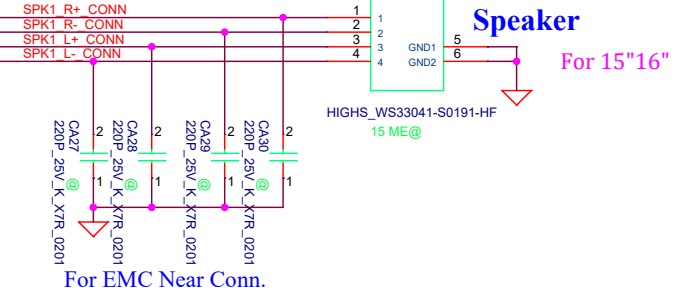
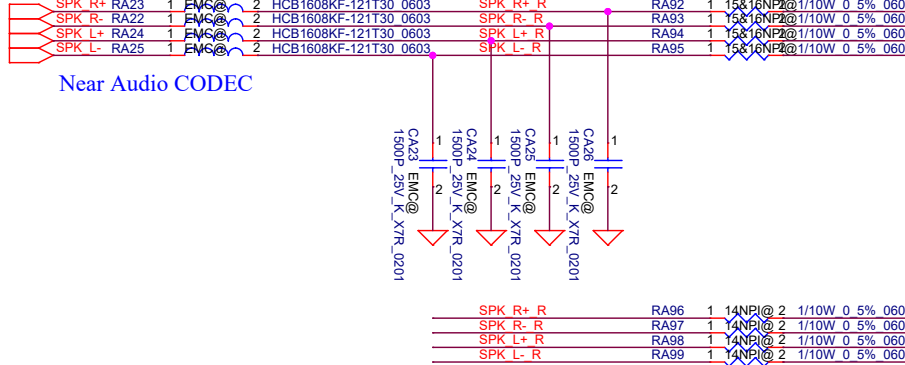


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				Date: Tuesday, January 03, 2023	Sheet 67 of 110	

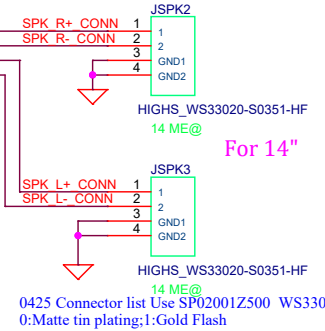


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					Date: Tuesday, January 03, 2023		Sheet 68 of 110

[66] SPK R+
[66] SPK R-
[66] SPK L+
[66] SPK L-

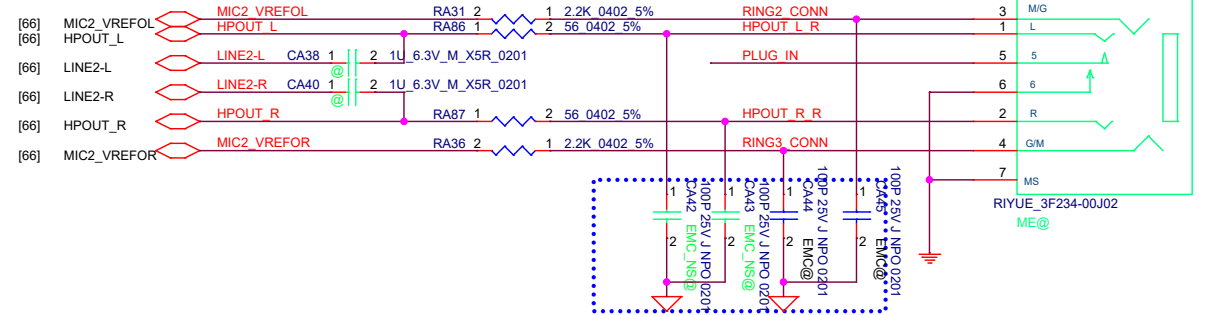
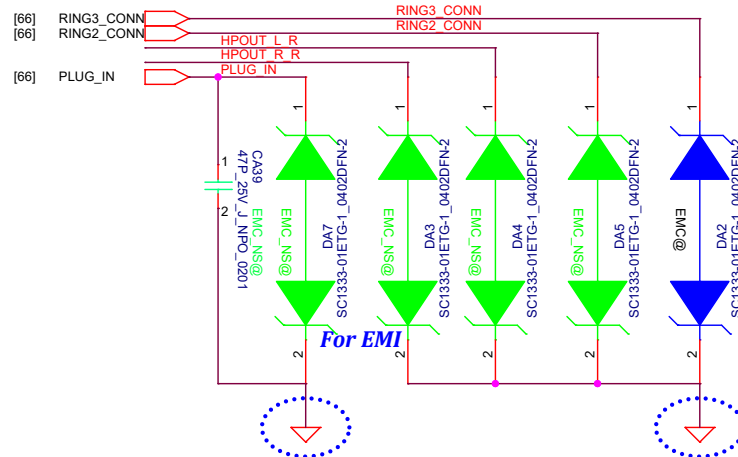
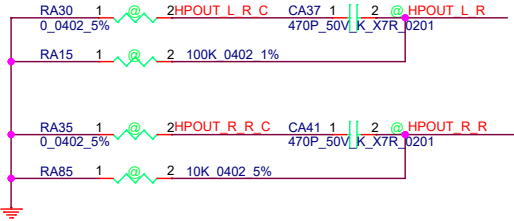


For EMC Near Conn.



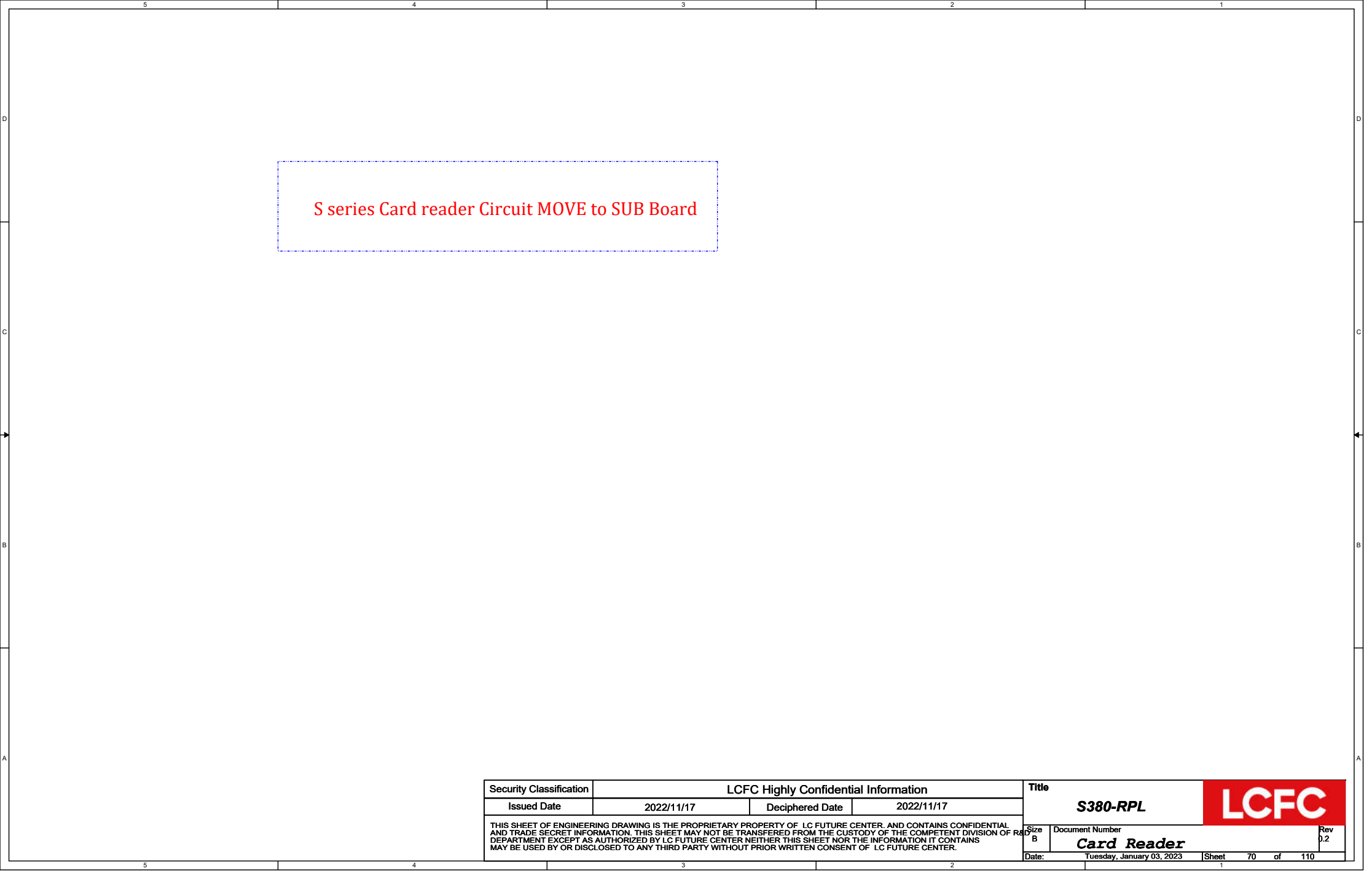
For EMC Near Conn.

EMC



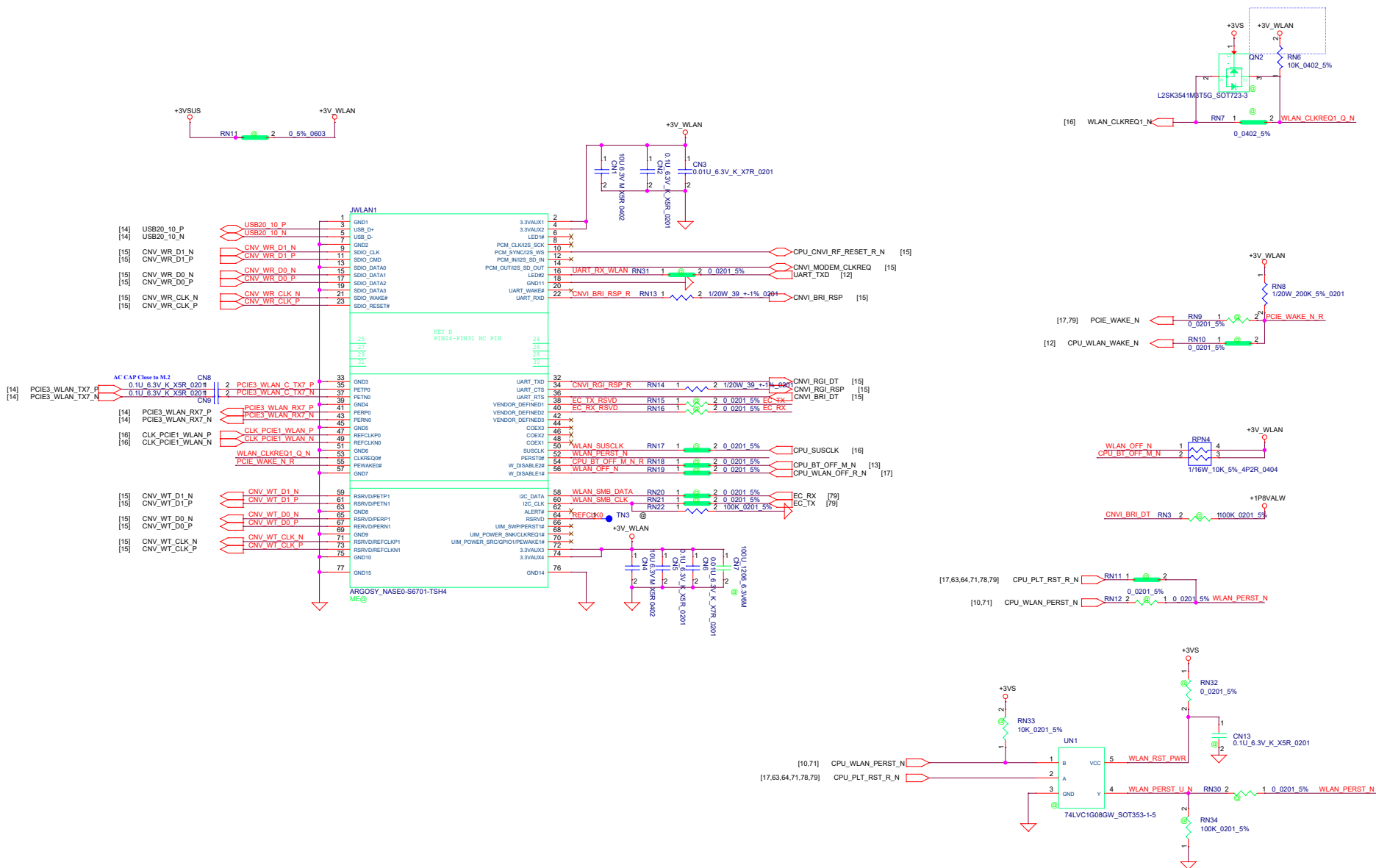
Audio Jack


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						B		Audio SPK/Jack		0.2	
						Date:		Tuesday, January 03, 2023		Sheet	

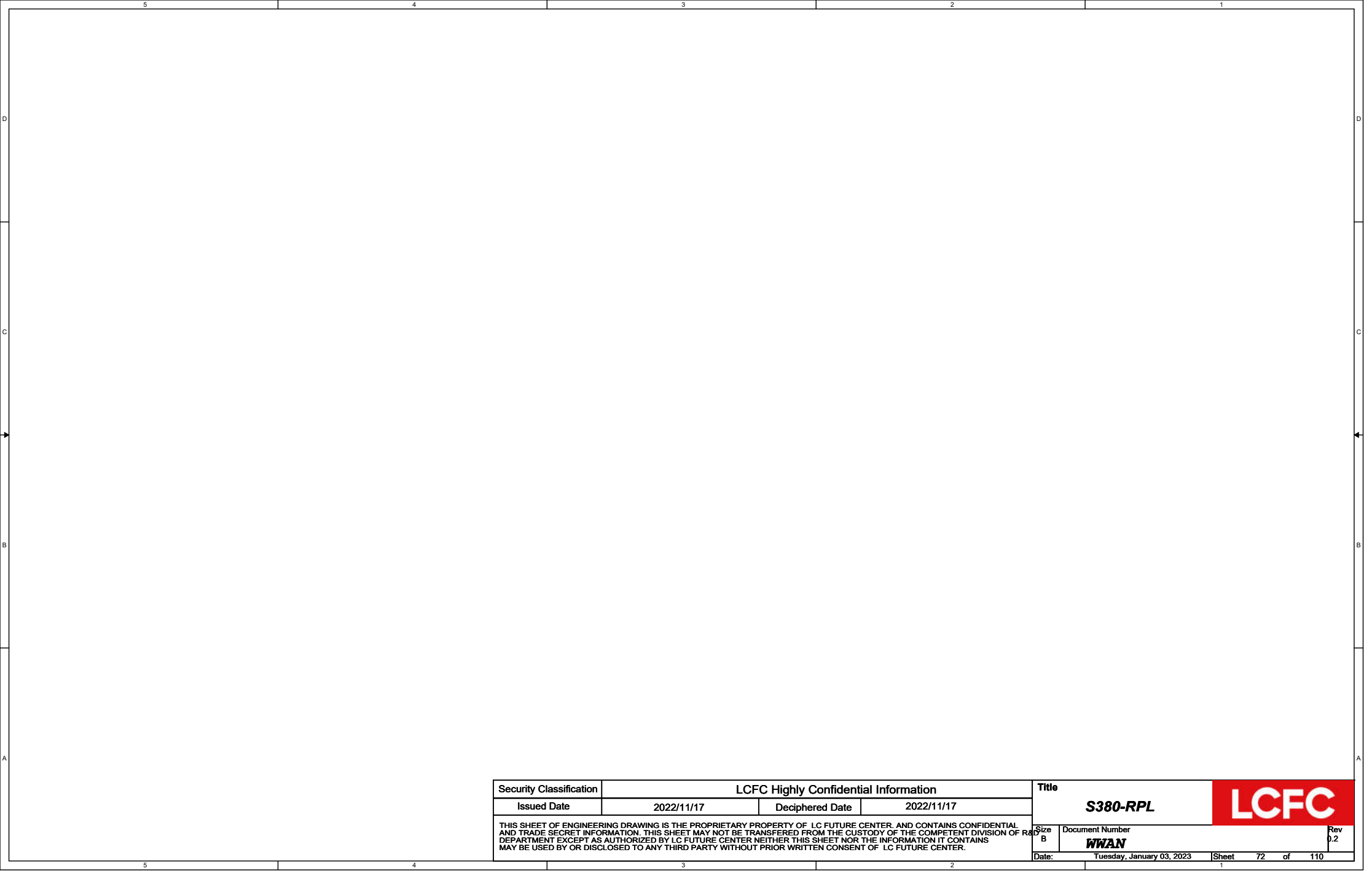


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Size		B		Document Number				Rev	
				Card Reader				0.2	
Date:		Tuesday, January 03, 2023				Sheet		70 of 110	

WLAN



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				Date:	Tuesday, January 03, 2023	Sheet 71 of 110



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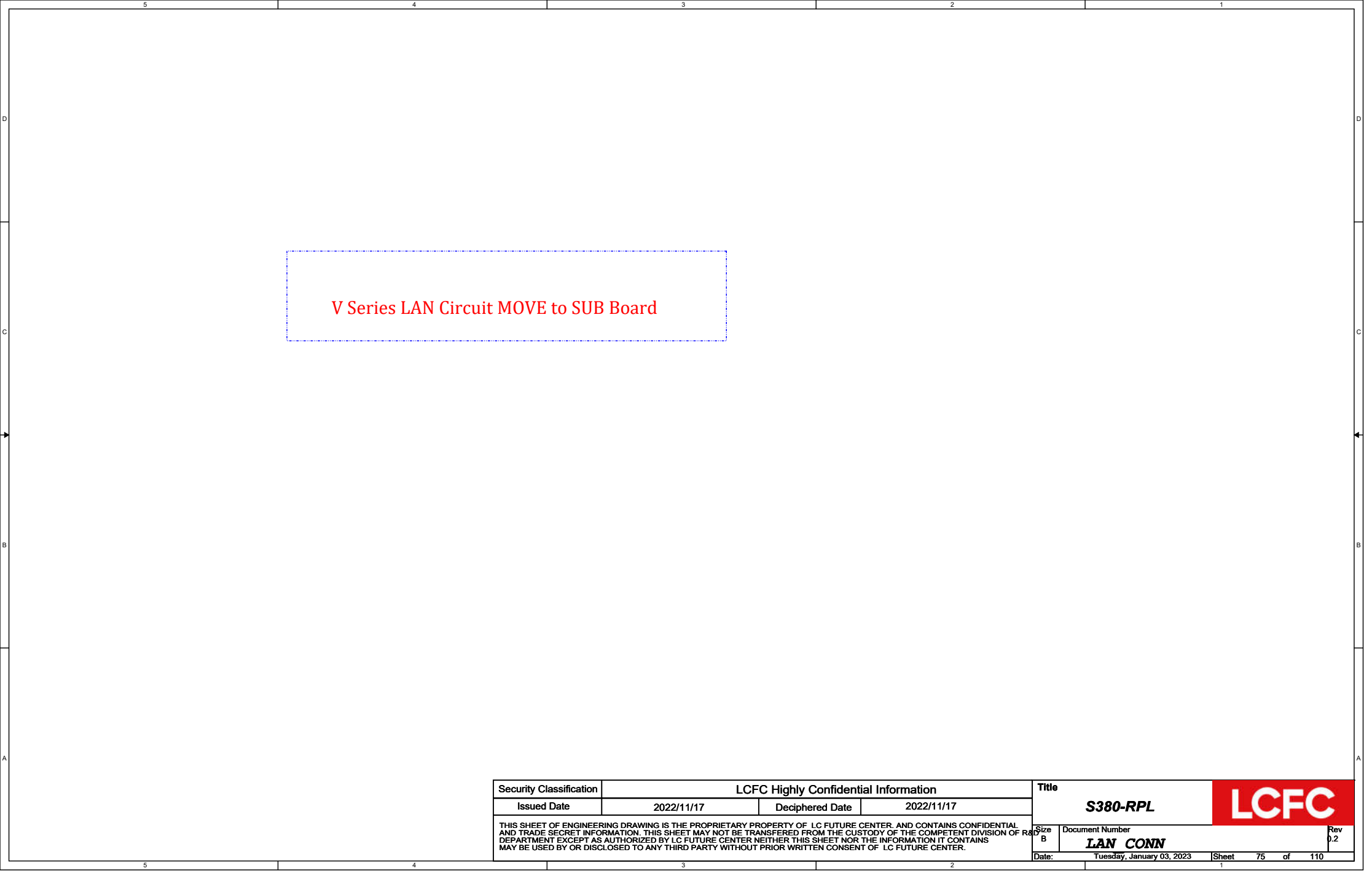
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Issued Date	2022/11/17	Deciphered Date	2022/11/17	S380-RPL			
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				Size B	Document Number WWAN	Rev 0.2	
				Date:	Tuesday, January 03, 2023	Sheet 72 of 110	

V Series LAN Circuit MOVE to SUB Board


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				Date:	Tuesday, January 03, 2023	Sheet 73 of 110

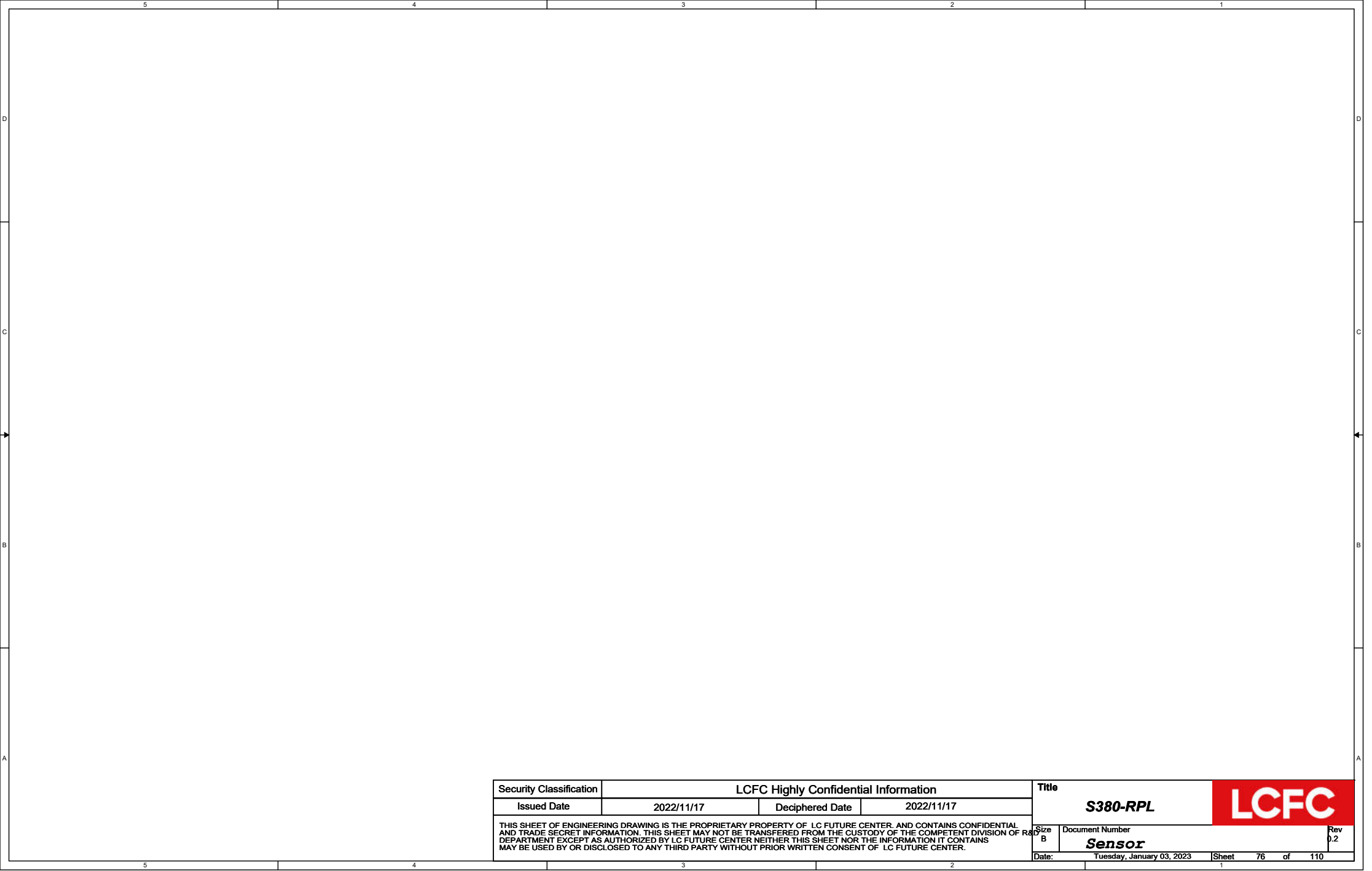
V Series LAN Circuit MOVE to SUB Board


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				B	LAN Transformer	0.2
				Date:	Tuesday, January 03, 2023	Sheet 74 of 110



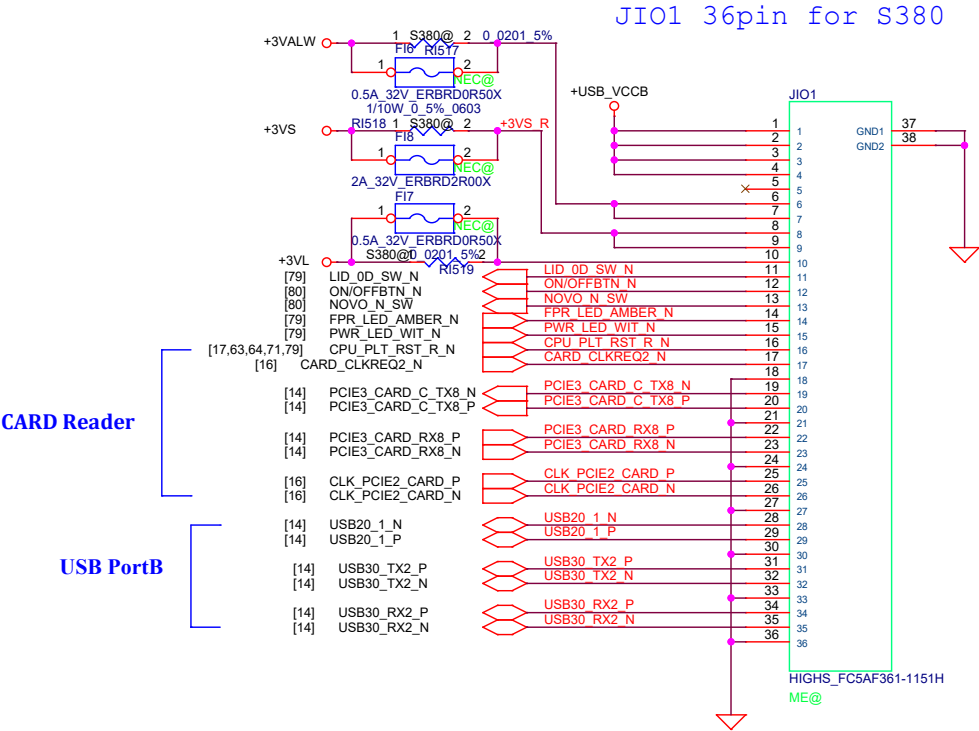
V Series LAN Circuit MOVE to SUB Board

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				Date: Tuesday, January 03, 2023		

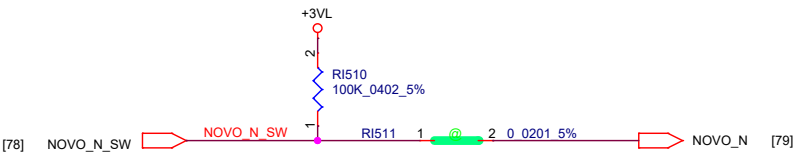


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				Date: Tuesday, January 03, 2023	Sheet 76 of 110	

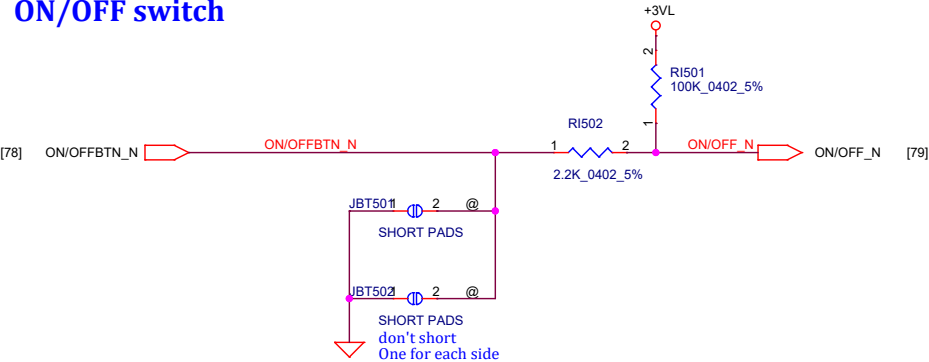
3VALW for V1415 POWER_LED&LAN CHIP Power; for S380 POWER_LED&FP_LED
3VS for V1415 Lan ISOLATE_N,for S380 Card Reader
3VL for Hall Sensor
LAN(LDO Mode);RTL8111H-CG :Isys(typical)=65+(150/0.33/3.3)=199.7mA
CR:OZ711LV2LN-A-0-TR :330mW
FP Module:45mA(Active)



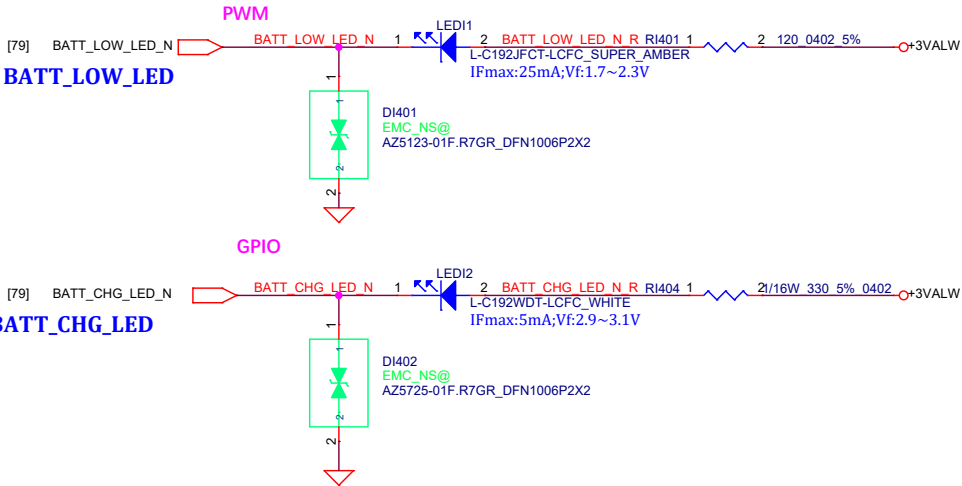
NOVO switch



ON/OFF switch



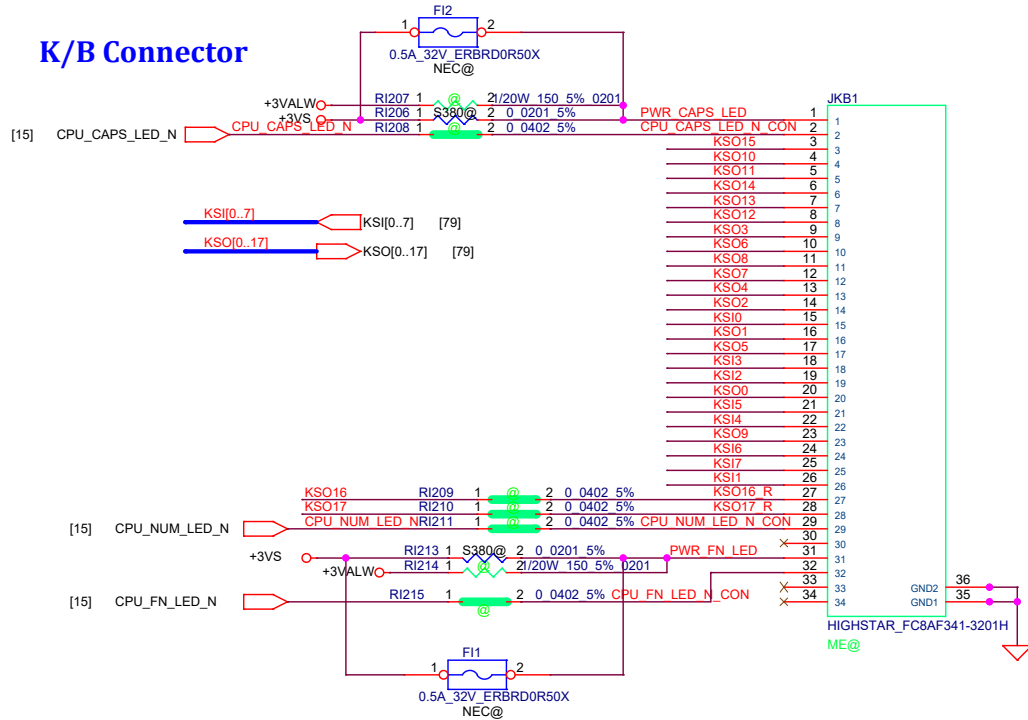
LED



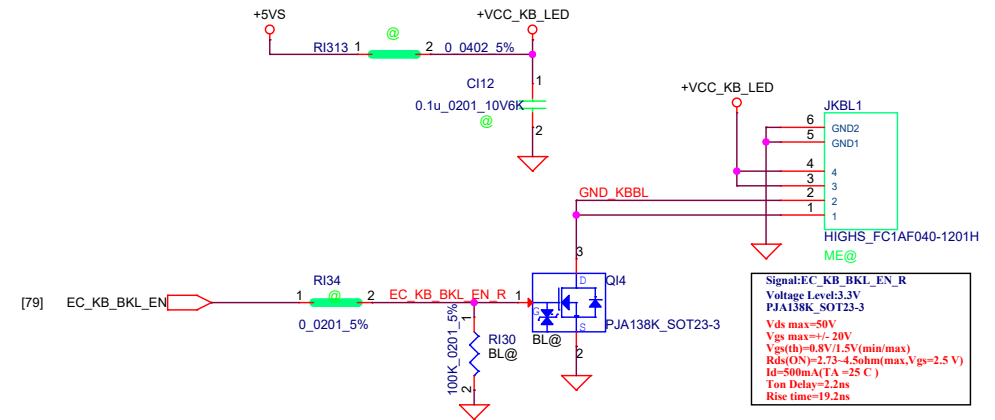
LED	Status	LED Behavior
Power Button	System on	White_on(battery: 21%~100%) Amber_on(battery: 0%~20%)
	Standby LID closed	White_on(battery: 21%~100%) Amber_Blink_3S(battery: 0%~20%)
	System off Battery only	OFF OFF
	Charging	Amber_on(battery: 1%~90%) White_on(battery: 91%~100%)

The Power LED move to SUB board LENS

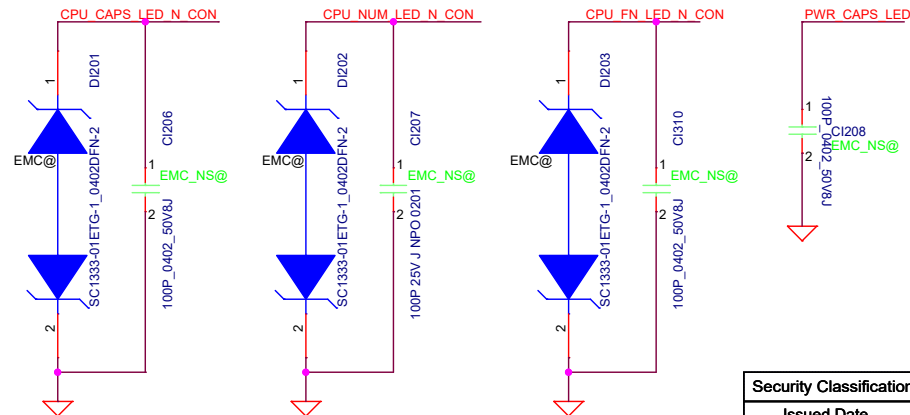
K/B Connector



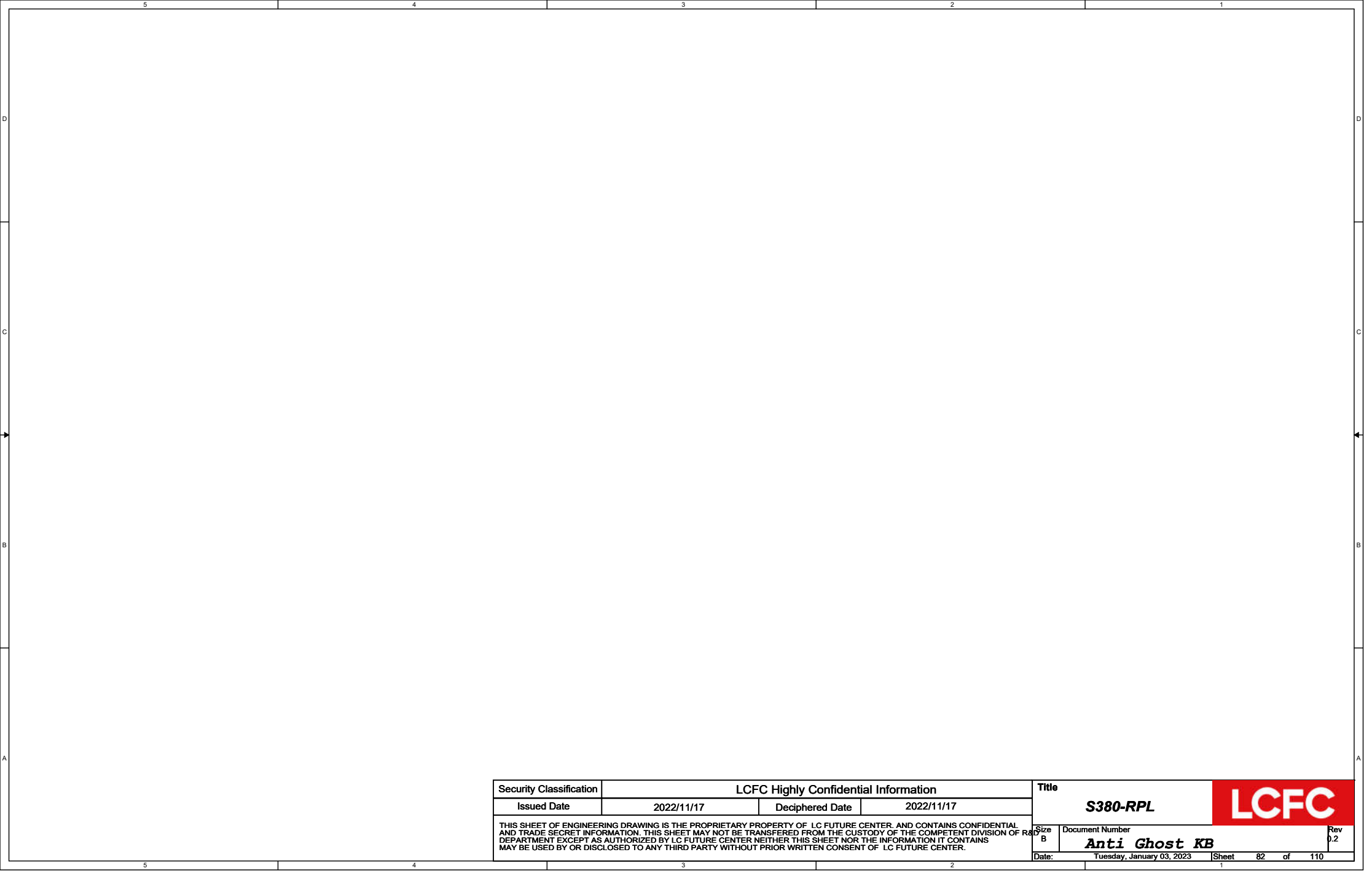
K/B Backlight Connector




EMC close to Conn

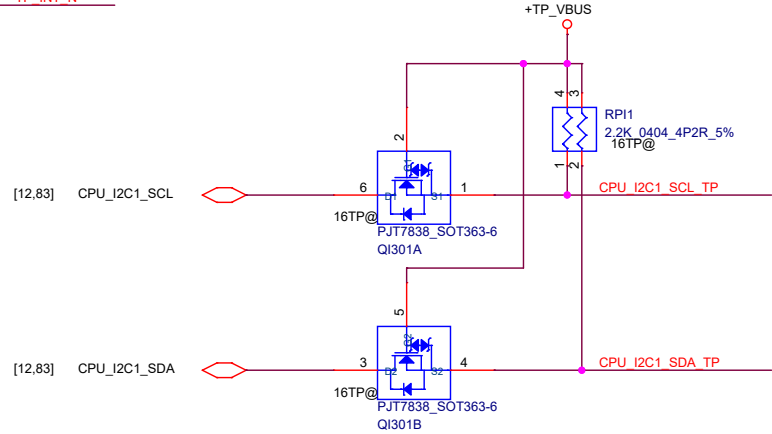
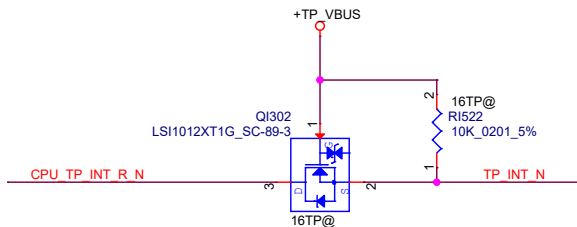
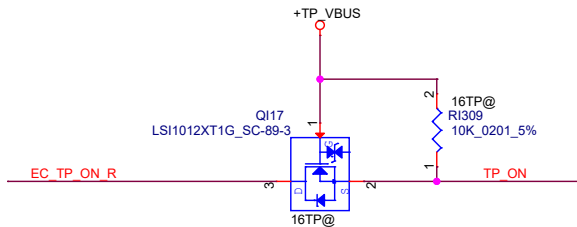
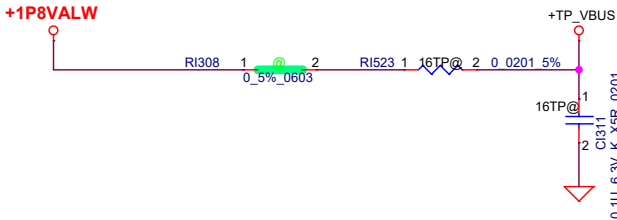
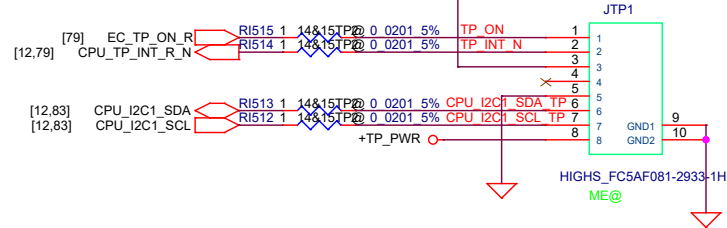
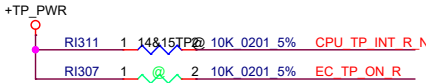
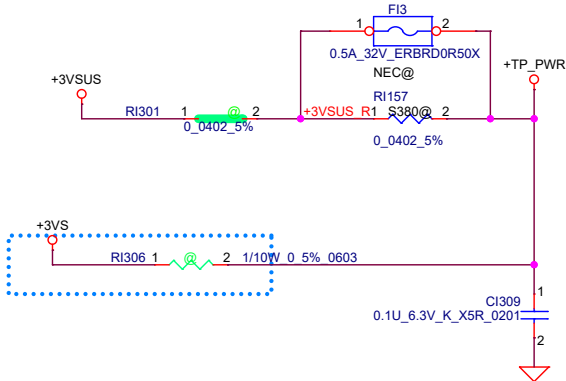


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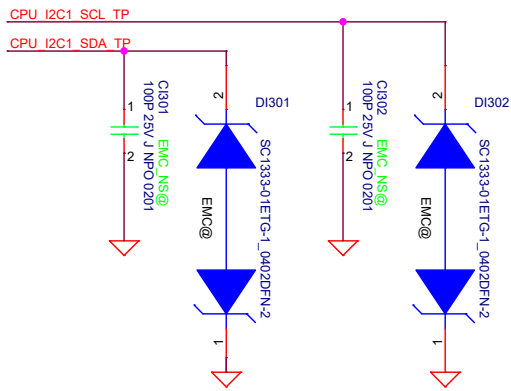



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				Size B	Document Number Anti Ghost KB	Rev 0.2	
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Touch Pad

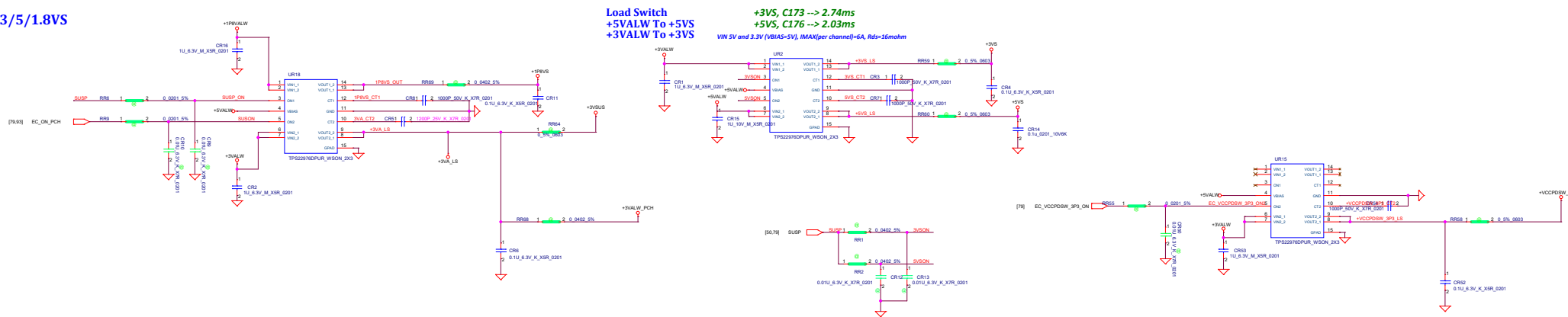


EMC close to Conn

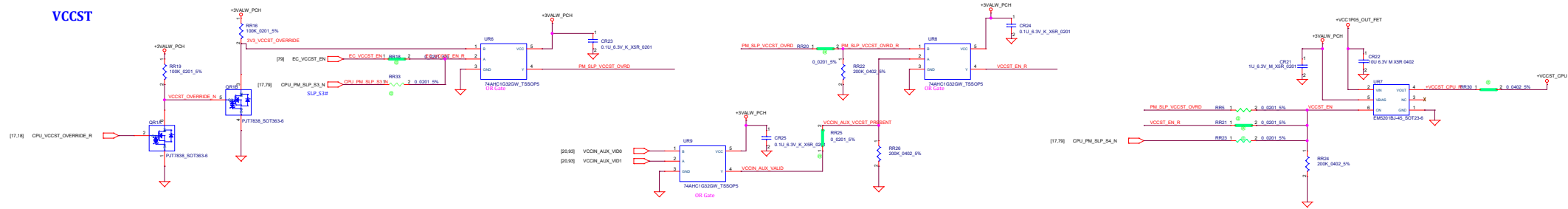


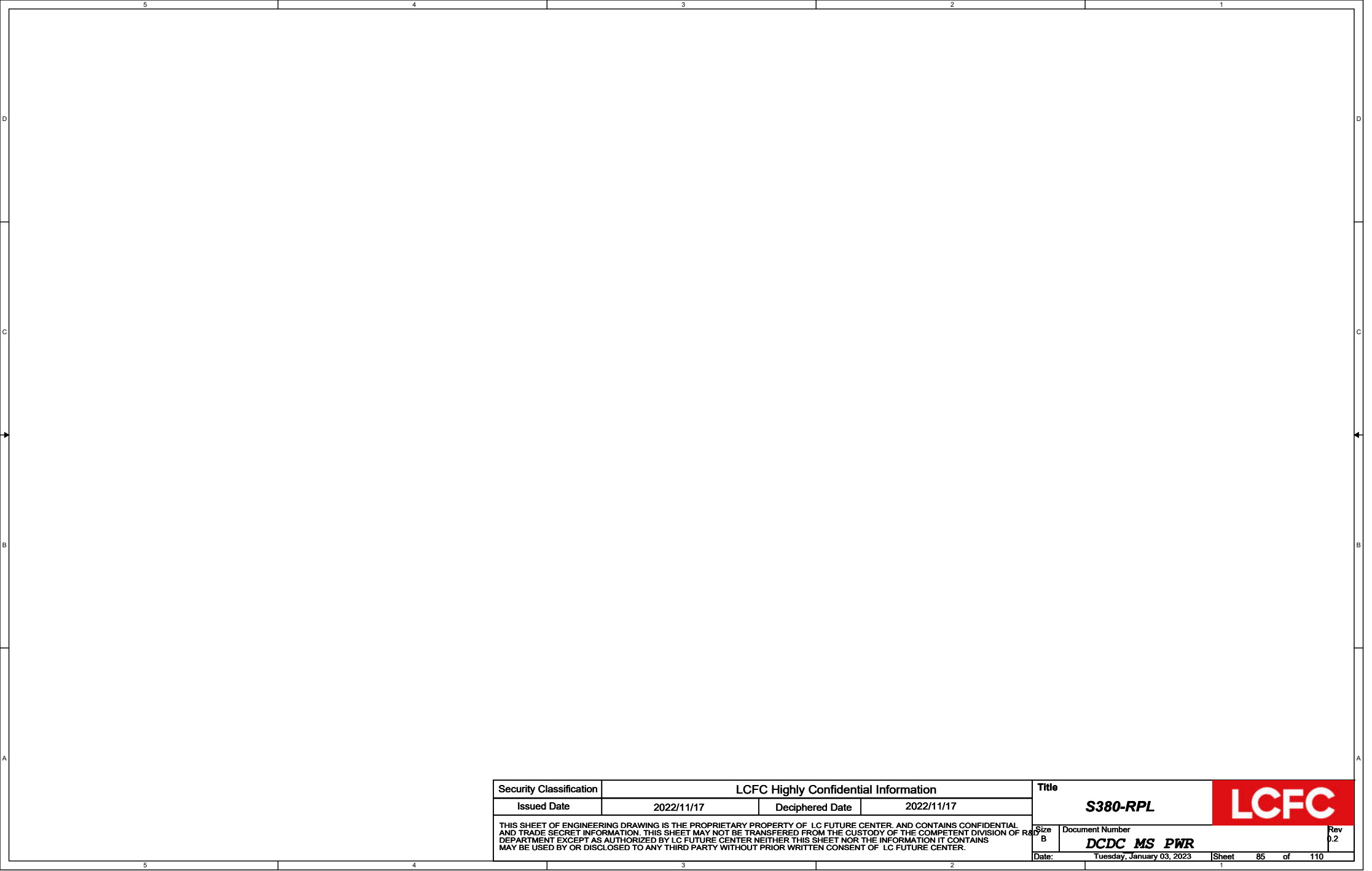
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						Size B		Document Number		Rev 0.2	
								TouchPad CONN			
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3/5/1.8VS

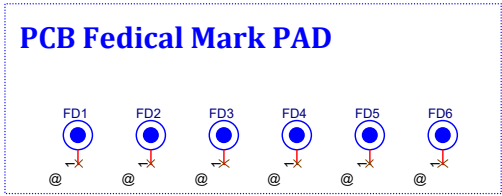


VCCST

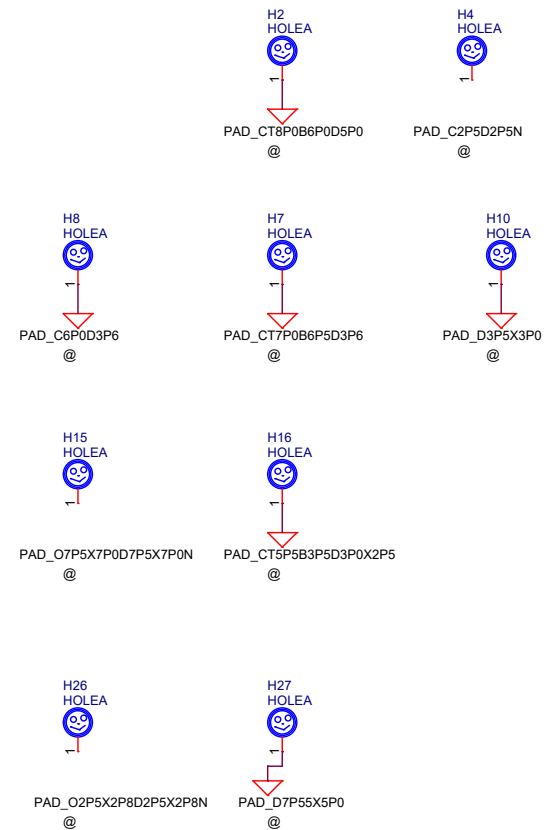




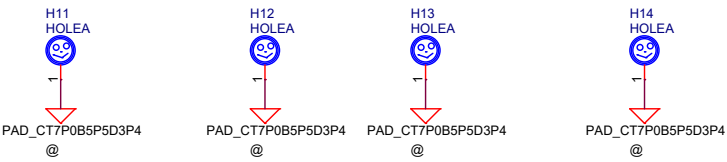
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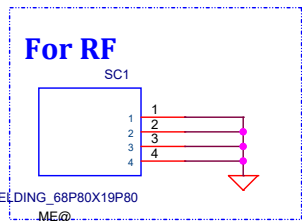
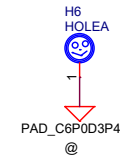
Hole



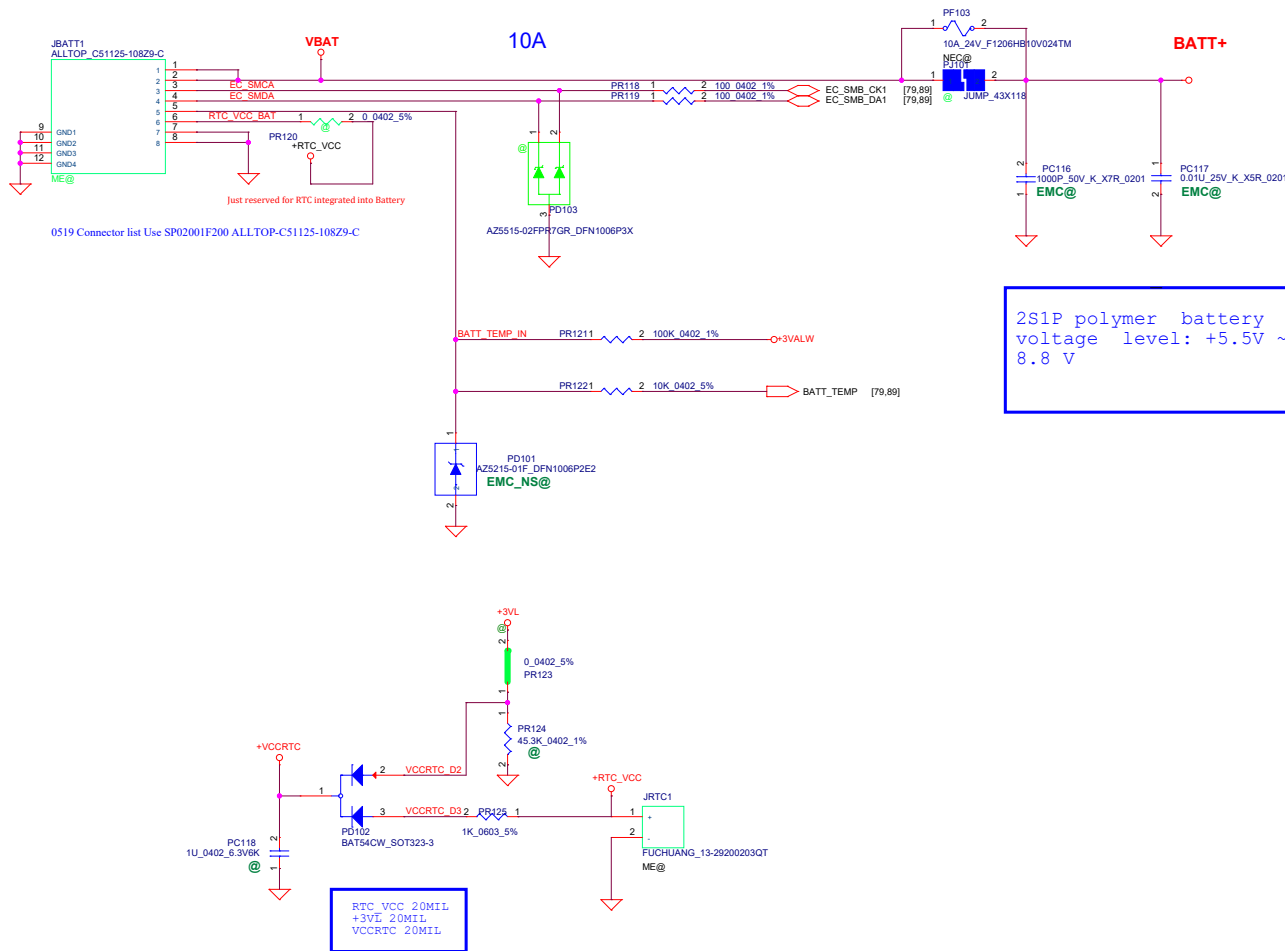
For Thermal

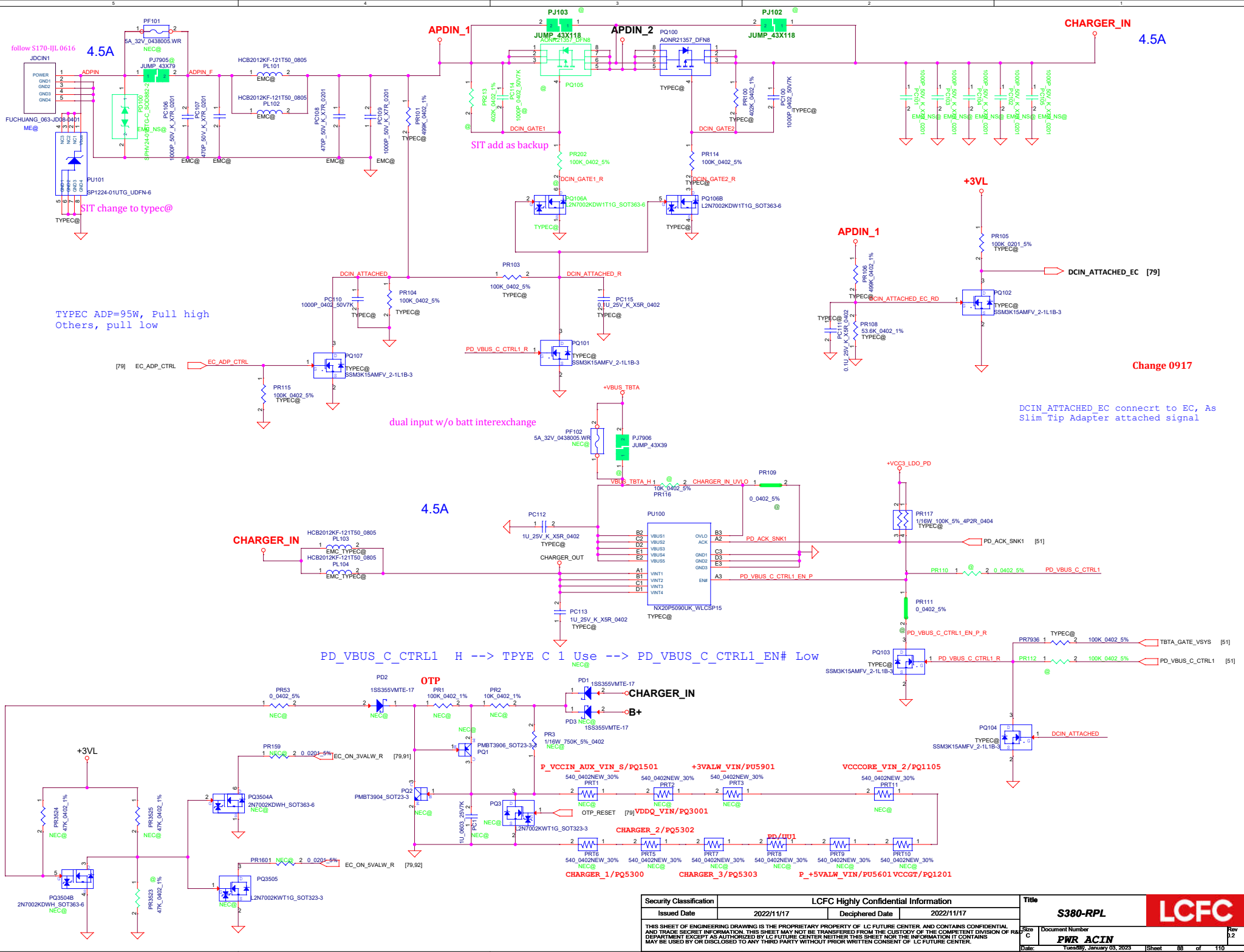


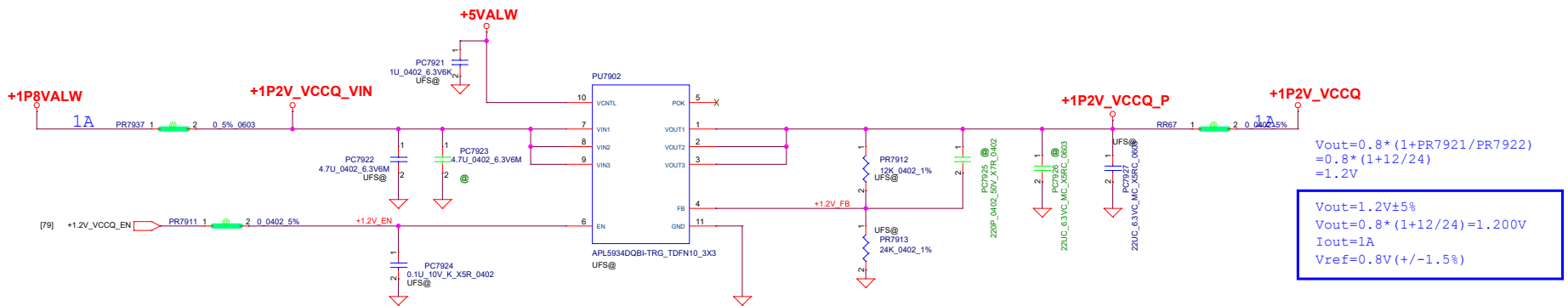
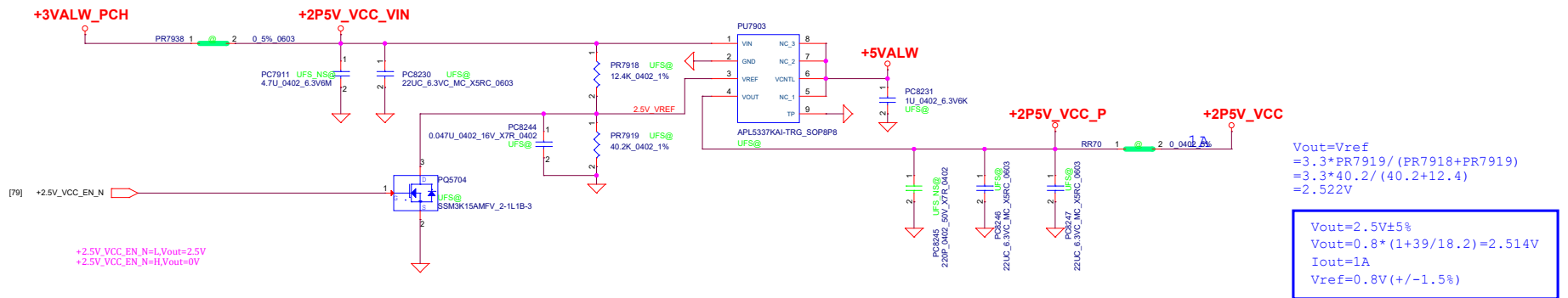
WLAN

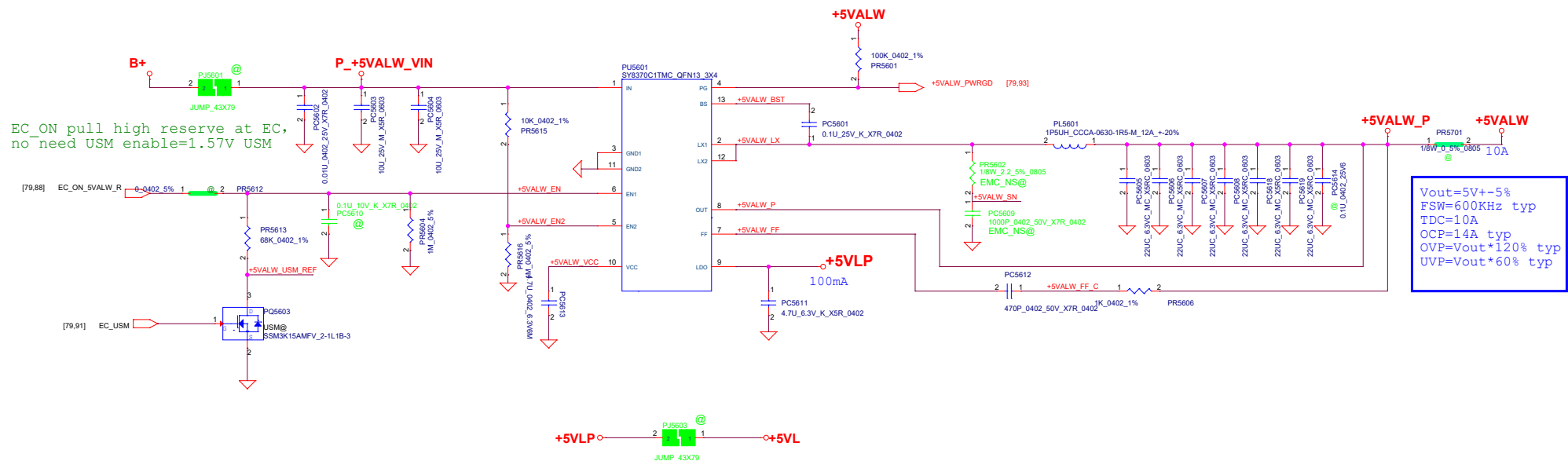


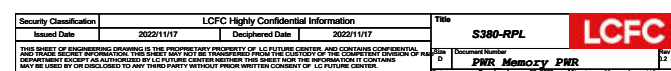
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		PHole/Shielding									
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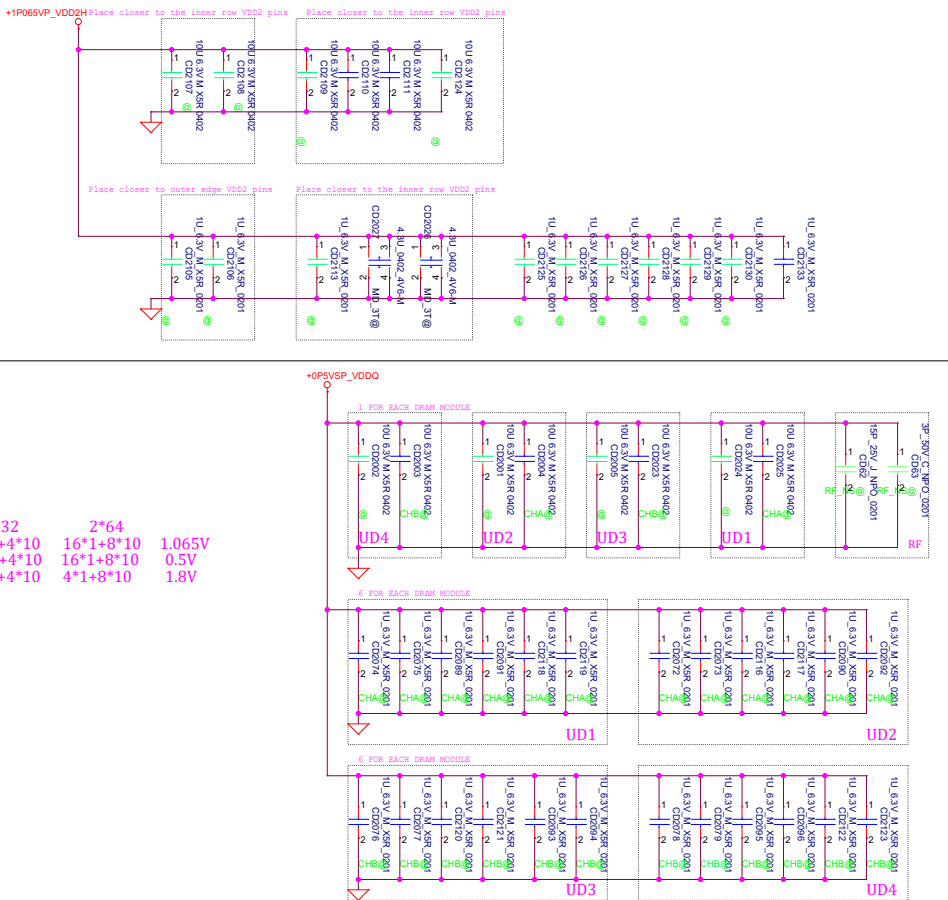
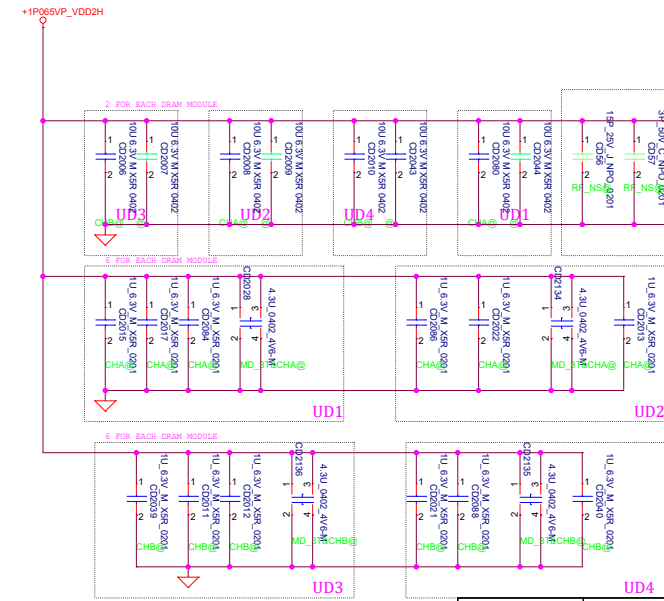
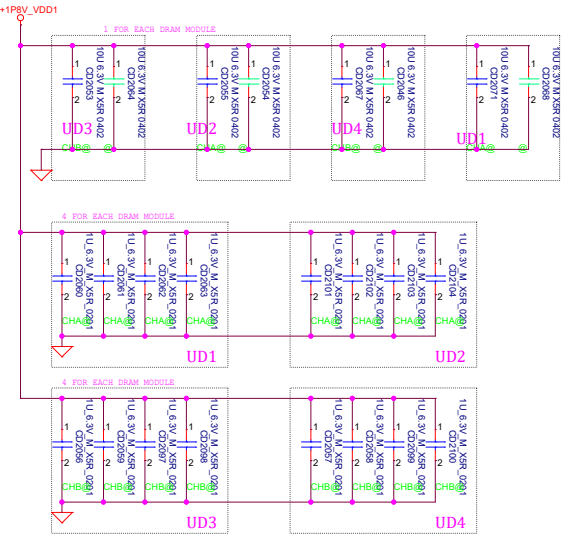


PDG CPU side:

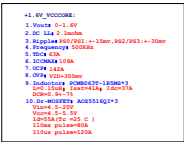
Voltage	Capacitor FF and Value	Quantity	Notes
VDD2(1.065V)	0402 1uF	2	Place closer to outer edge VDD2 pins
VDD2(1.065V)	0402 placeholder	2	Place closer to the inner row VDD2 pins
VDD2(1.065V)	0402 10uF	3	Place closer to the inner row VDD2 pins
VDD2(1.065V)	0402 1uF	4	Place closer to the inner row VDD2 pins

PDG Memory Down:

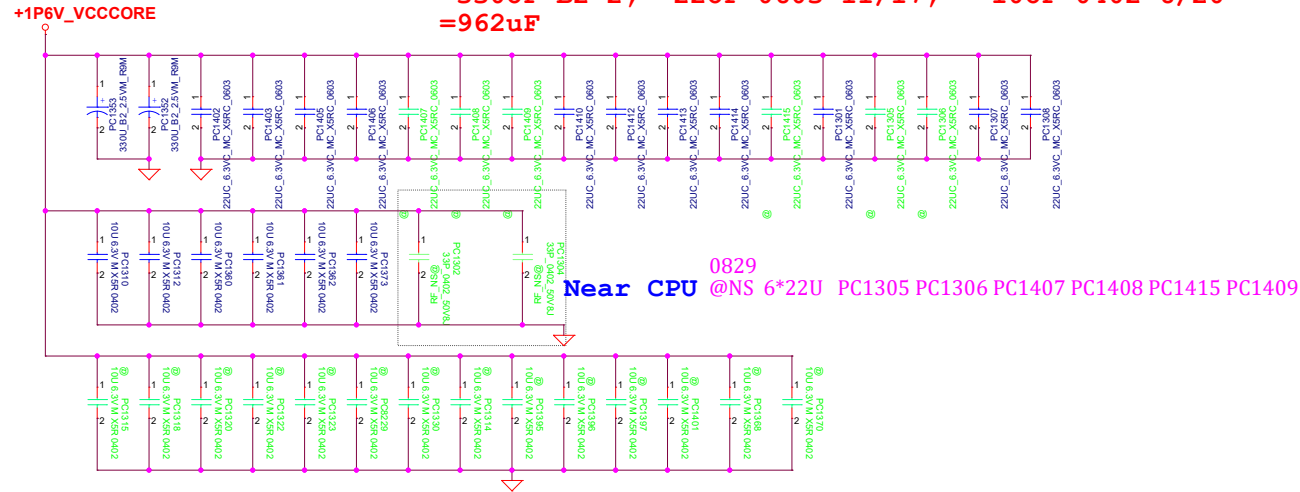
Voltage	Capacitor FF and Value	Quantity	Notes
VDD2(1.065V)	0402/0201 1uF	24	6 caps per DRAM, 2 per short edge and 1 per long edge close to VDD2H/VDD2L BGA's
VDD2(1.065V)	0603/0402 10uF	4	evenly distribute among all DRAMs
VDDQ(0.5V)	0402/0201 1uF	24	6 caps per DRAM, 2 per edge close to VDDQ BGA's
VDDQ(0.5V)	0603/0402 10uF	4	evenly distribute among all DRAMs Customers may adjust the Capacitor Quantity/FF/Value to meet the JEDEC SPEC
VDD1(1.8V)	0402/0201 1uF	16	4 caps per DRAM, 2 per long edge close to VDD1 BGA's Customers may adjust the Capacitor Quantity/FF/Value to meet the JEDEC SPEC
VDD1(1.8V)	0603/0402 10uF	4	evenly distribute among all DRAMs Customers may adjust the Capacitor Quantity/FF/Value to meet the JEDEC SPEC



LPDDR5 4*32 2*64
VDD2 24*1+4*10 16*1+8*10 1.065V
VDDQ 24*1+4*10 16*1+8*10 0.5V
VDD1 16*1+4*10 4*1+8*10 1.8V

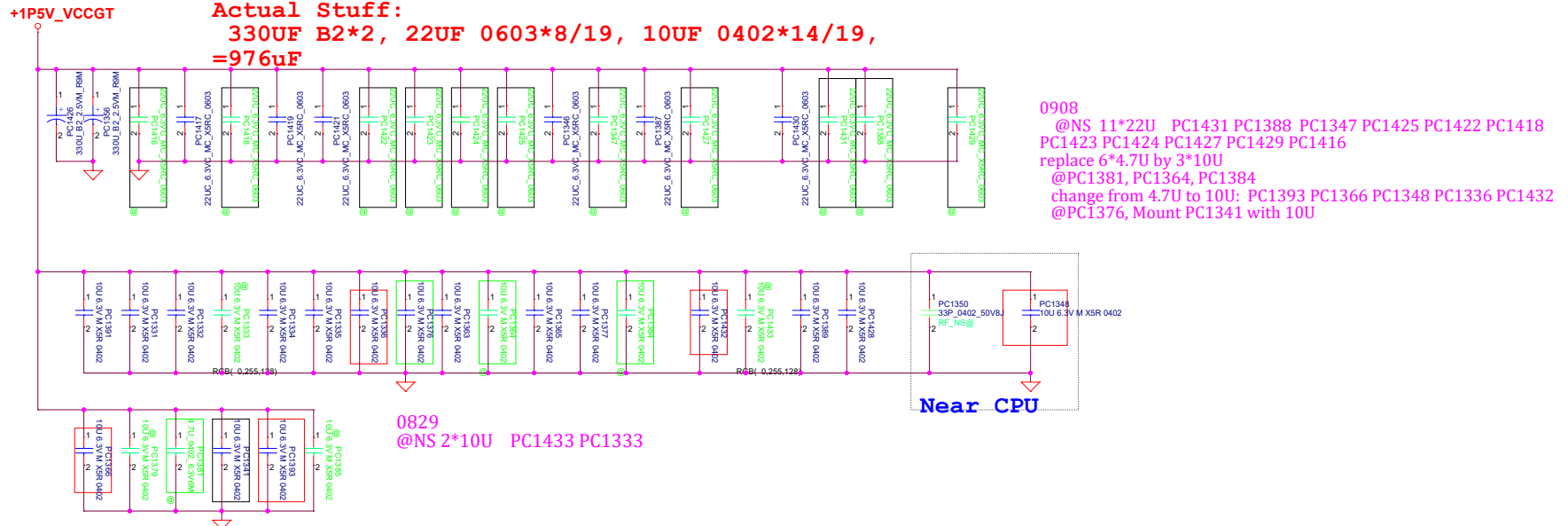


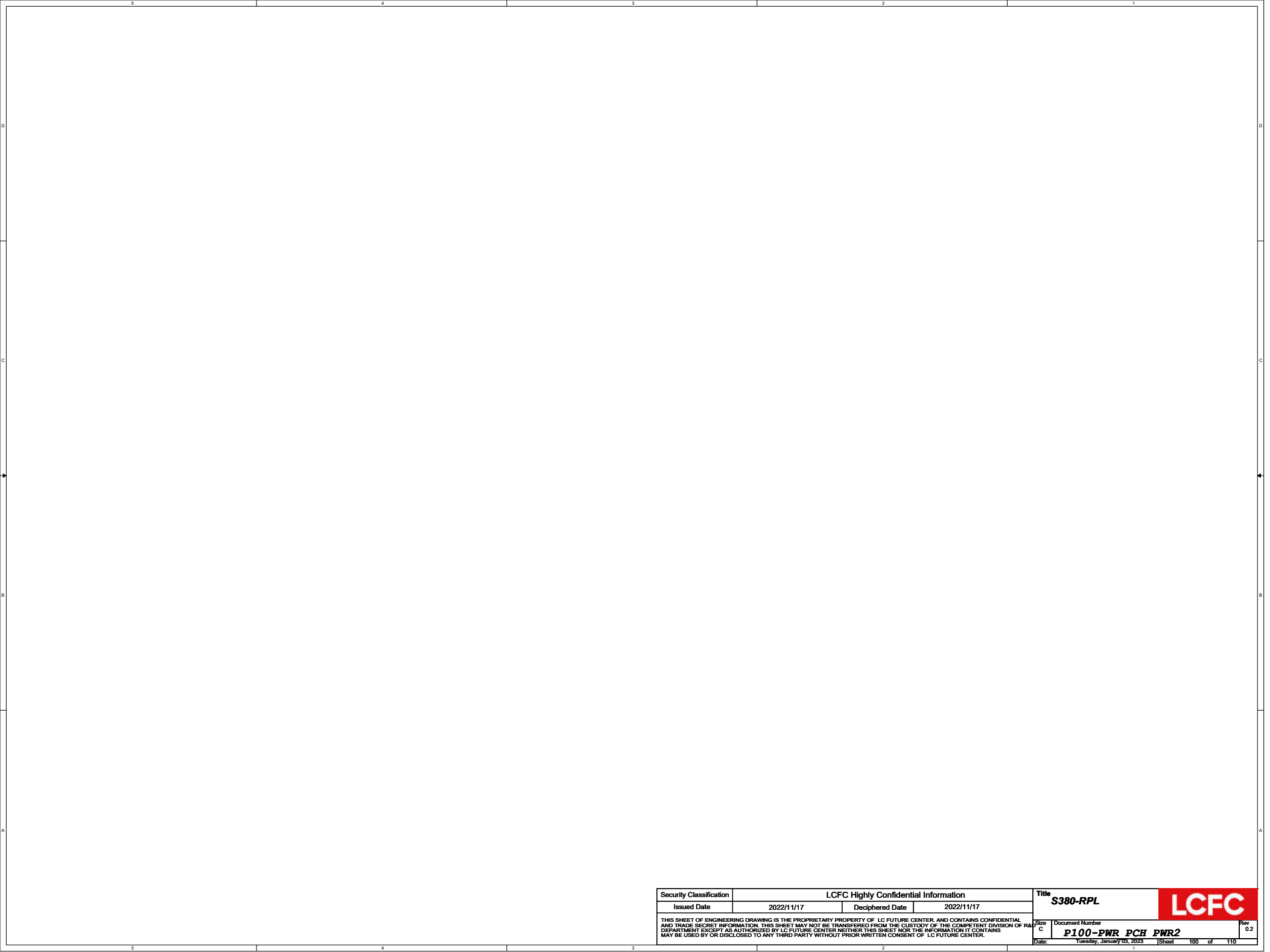
Actual Stuff:
330UF B2*2, 22UF 0603*11/17, 10UF 0402*6/20
=962uF



Follow PDG v0.7
15W:330uF 7343 2pcs, 47uF 0603 7/8pcs, 22uF 0402 8pcs, 10uF 0402 2/4pcs
=1185uF

Actual Stuff:
330UF B2*2, 22UF 0603*8/19, 10UF 0402*14/19,
=976uF



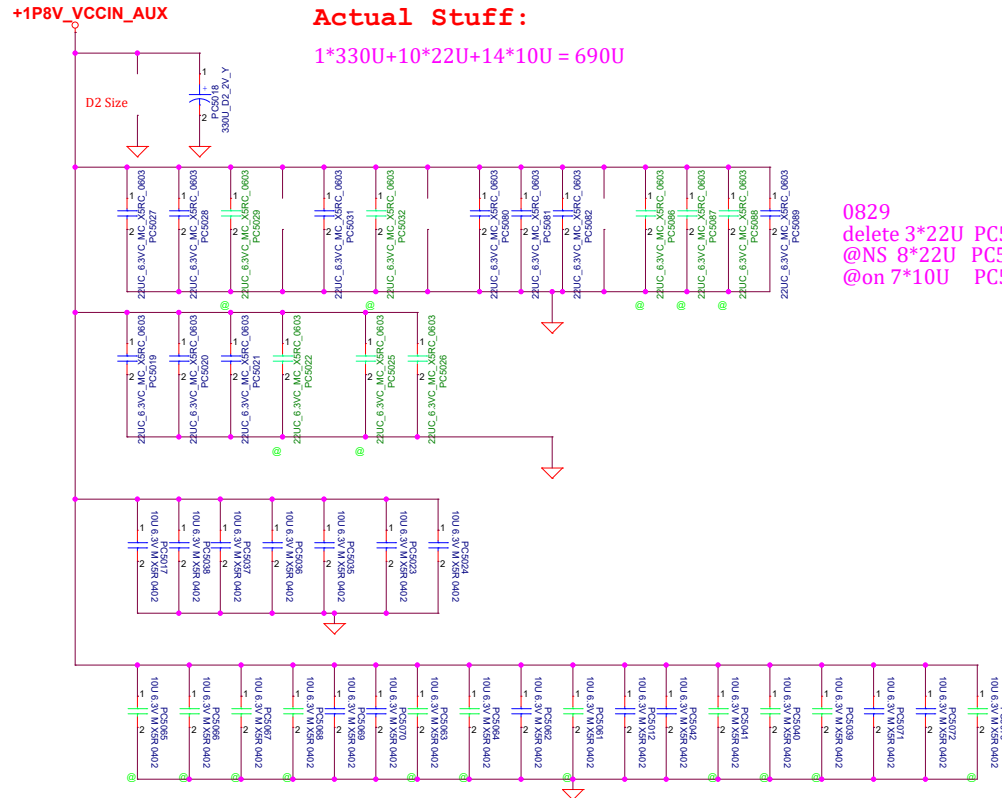


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Size C				Document Number	
Date				P100-PWR PCH PWR2	
1				Rev 0.2	
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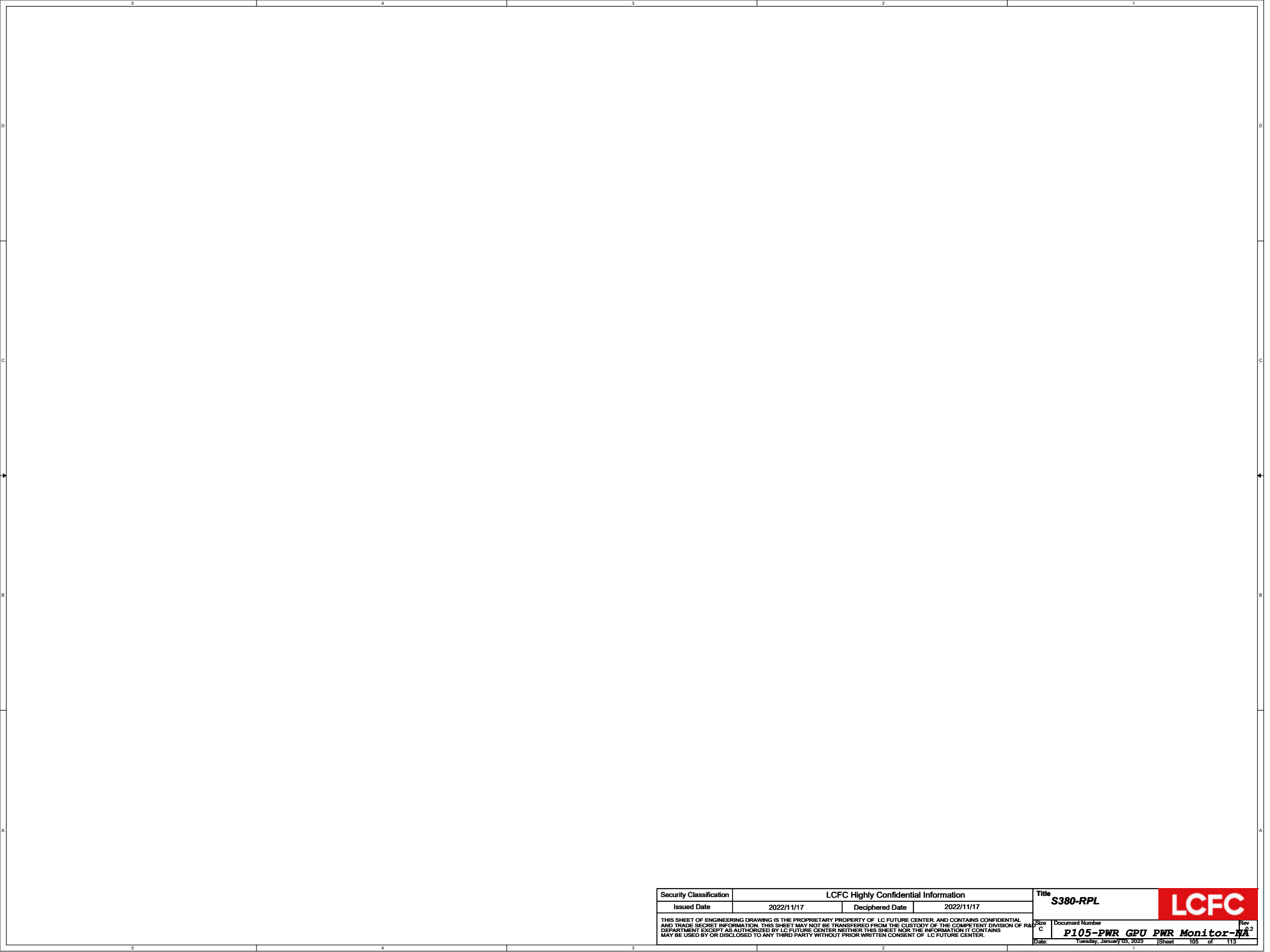
Follow PDG v0.7:
330uF 7343 1pcs, 47uF 0603 9pcs, 10uF 10/11pcs
=853uF


Actual Stuff:

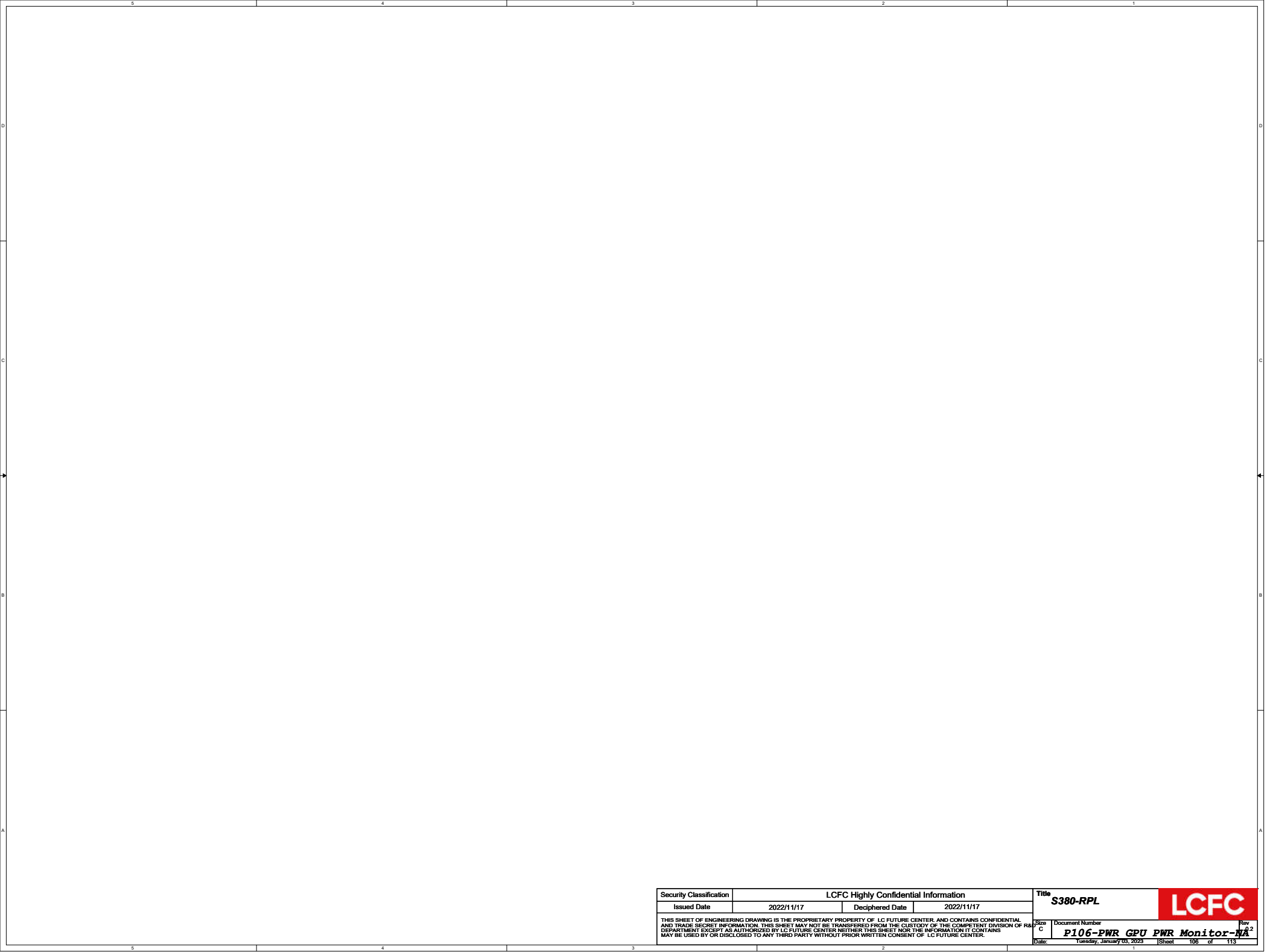
1*330U+10*22U+14*10U = 690U




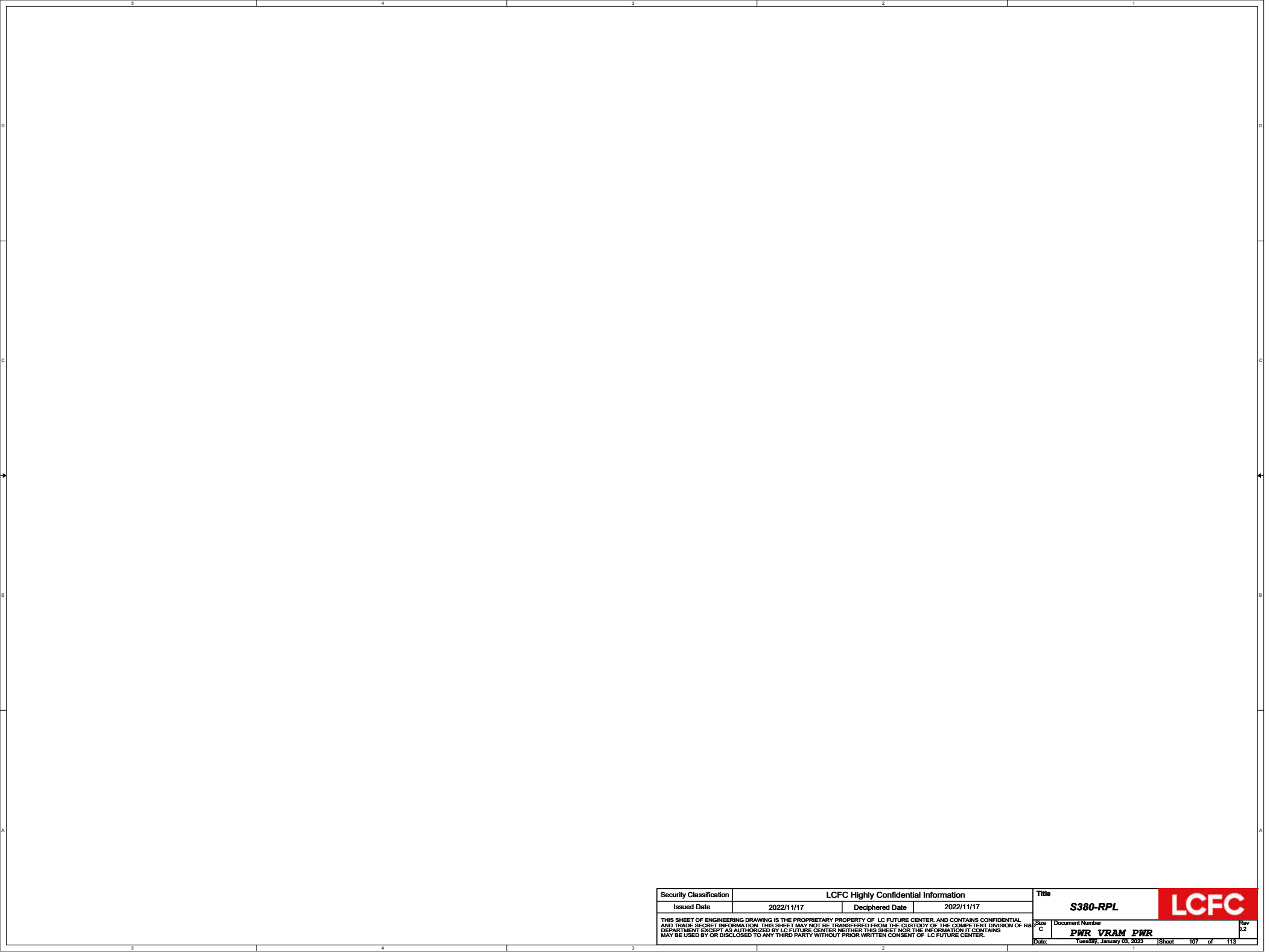
0829
delete 3*22U PC5030 PC5033 PC5085
@NS 8*22U PC5022 PC5025 PC5026 PC5029 PC5032 PC5086 PC5087 PC5088
@on 7*10U PC5069 PC5070 PC5071 PC5072 PC5042 PC5062 PC5012



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Size		C		Document Number		P106-PWR GPU PWR Monitor-NA		Rev 02	
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					PWR VRAM PWR
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Change List

- 1.TP 针对16吋SKU，更正线路图。增加TP_ON/TP_INT电路level shifter电路。更正RI514/RI515 BOM structure。
- 2.新增P79，对EC_VCCPDSW_3P3_ON_R信号经100K电阻pull high 到+3VALW
- 3.CC10/CC11电容容值从10P更改成12P
- 4.H28 封装更改
- 5.P79 更改EC_ON_PCH_R上拉电压为3VALW



- 1.del PR2059
- 2.ADD PC5075,PC5076
- 3.GPU PWR conntroller VCC PVCC change to +5VS,PR2060 stuff,PR2061 no stuff
- 4.DCIN_ATTACHED_EC change to pull high to +3VL ,PQ202 SWAP,PR206 change to 499K
- 5.PR2214 change to 0 ohm
- 6.ADD PC2110, ADD PR2062,PR2063,PR2041 ,PR2045change to 698ohm
- 7.PR2031 change to 23.7K,PR2032 change to 12.7K
PR2033 change to 16.9K,PR1068 change to31.6K
PR1069 change to 26.7K,PC1015 change to 56PF
PR1078 change to 10.5K,PR2039 change to 30.1K
PR2056 change to 73.2K,PR2058 change to 100K
CG2717,CG2718,CG3671,CG3672 stuff
- 8.CPU power电感换2.4mm高的sample: PL1101,PL1102,PL1201,PL1501并增加相应的short pin
- 9.非core power的电感主料换Coilforce的PN(PL6502,PL3001,PL5701,PL5400,PL5601)
- 10.PQ 1102,PQ1104,PQ1106,PQ1108,PQ1202,PQ1204,PQ1502 change to AON6324

2022/02/08
1.PJ2201 Change to PL2202

- 11/23
- 1.PR2033 16.9K change to 11.3K
PR2031 23.7K change to 21K
PR2032 12.7K change to 15.4K
PR2039 30.1K change to 95.3K
PC2005 220P change to 150pF
PR2028 470 change to 402R
PR2015 2.37K change to 6.19K
PR2024 1K change to 3.32K
PR2027 442 change to 49.9R

- 11/25
- 1.PC2202,PC2224,PC4002,PC4003,PC4019,PC4020,
PC5494,PC5495,PC5601,PC5604,PC5703,PC5704
change to SE000010U00
- 2.Delete PJ1501,PJ1100,PJ1101,PJ1200 ,delete PD2000

- 12/13
- 1.P103: delete PJ2101,ADD PR2130,PR2131,ADD PU2102及其周边相关电阻电容,
- 2.P104: 20VB+ change to20VB+_GPU

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D

C

B

A

D

C

B

A

Resistor (1%)	SMBus Address
0 (Tie to GND)	0010_000(x/v)
499	0010_001(x/v)
806	0010_010(x/v)
1,270	0010_011(x/v)
2,050	0010_100(x/v)
3,240	0010_101(x/v)
5,230	0010_110(x/v)
8,450	0010_111(x/v)
13,300	0011_000(x/v)
21,500	0011_001(x/v)
34,000	0011_010(x/v)
54,900	0011_011(x/v)
88,700	0011_100(x/v)
140,000	0011_101(x/v)
226,000	0011_110(x/v)
Tie to V _{DD}	0011_111(x/v)

USB2.0
I2C

SEL	OE	Y+	Y-
X	H	H _h -Z	H _h -Z
L	L	M+	M-
H	L	D+	D-

